

Anisotropic viscoelastic shell modeling technique of copper patterns/photoimageable solder resist composite for warpage simulation of multi-layer printed circuit boards

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2015 J. Micromech. Microeng. 25 105016

(<http://iopscience.iop.org/0960-1317/25/10/105016>)

View [the table of contents for this issue](#), or go to the [journal homepage](#) for more

Download details:

IP Address: 166.104.75.38

This content was downloaded on 16/09/2015 at 01:45

Please note that [terms and conditions apply](#).

Anisotropic viscoelastic shell modeling technique of copper patterns/photoimageable solder resist composite for warpage simulation of multi-layer printed circuit boards

Do-Hyoung Kim¹, Sung-Jun Joo¹, Dong-Ok Kwak² and Hak-Sung Kim^{1,3}

¹ Department of Mechanical Engineering, Hanyang University, Haengdang-dong, Seongdong-gu, Seoul 166-791, Korea

² Memory Division, Samsung Electronics, Hwasung-si 445-701, Korea

³ Institute of Nano Science and Technology, Hanyang University, Seoul, 133-791, Korea

E-mail: kima@hanyang.ac.kr

Received 11 May 2015, revised 25 July 2015

Accepted for publication 10 August 2015

Published 15 September 2015



Abstract

In this study, the warpage simulation of a multi-layer printed circuit board (PCB) was performed as a function of various copper (Cu) patterns/photoimageable solder resist (PSR) composite patterns and their anisotropic viscoelastic properties. The thermo-mechanical properties of Cu/PSR patterns were obtained from finite element analysis (virtual test) and homogenized with anisotropic composite shell models that considered the viscoelastic properties. The multi-layer PCB model was simplified based on the unit Cu/PSR patterns and the warpage simulation during the reflow process was performed by using ABAQUS combined with a user-defined subroutine. From these results, it was demonstrated that the proposed anisotropic viscoelastic composite shell simulation technique can be successfully used to predict warpage of multi-layer PCBs during the reflow process.

Keywords: printed circuit board (PCB), warpage simulation, viscoelastic property, anisotropic shell model

(Some figures may appear in colour only in the online journal)

1. Introduction

Warpage of printed circuit boards (PCBs) can cause significant problems during manufacturing processes and reduce the reliability of the product. Many problems have been reported including damage and mismatching of components, disconnection of solder paste bridging, cracking of solder joints, and line jams during production [1–4]. Nowadays, it has become critically important to design electronic devices that are lighter and smaller in size. In many electronic products, such as smart phones, solid state disks (SSDs), or multimedia cards (MMC), there is an increasing desire for devices to

be lighter, smaller, and have more functionality. Therefore, PCBs should be designed with extremely finer electrode lines, higher circuit density, and thinner cross-sections. Also, multi-layer PCBs are used extensively to integrate more chips. Therefore, the relative impact of warpage on electronic products has increased [3, 5]. For these reasons, the warpage of multi-layer PCBs must be accurately predicted and controlled to improve the reliability of electronic product components.

The warpage of PCBs is generated by several factors such as temperature changes in the manufacturing process, moisture absorption, and mechanical load. Among

them, thermally-induced warpage, which leads to thermo-mechanical deformation during high temperature reflow processes, is the most prevalent [1]. Typically, a multi-layer PCB is composed of various materials such as a woven glass fabric/bismaleimide triazine epoxy composite film substrate (BT-core), copper (Cu), and photoimageable solder resists (PSRs). Therefore, different amounts of thermal expansion in each layer are caused by the structural differences of copper circuit and mismatched thermal expansion (CTE) values of each materials. This results in thermally-induced warpage during the high temperature reflow processes.

To predict thermal warpage in PCBs, several studies have used numerical analysis to consider the layer structure and material characteristics [6–8]. Numerical homogenization of Cu traces has been performed in many studies because the Cu circuits in microelectronic substrates are too small and too complicated to model each individual copper pattern with a simulation model. For this reason, PCBs have been represented by isotropic models [9–11] or as plates with orthotropic elastic mechanical properties [12–15]. However, in these previous works, only the copper line patterns were considered; other Cu patterns formed by various shapes, such as dummy, grid, circular, or square pads, were neglected. However, these additional patterns should be considered in the homogenization procedure of the PCB area because experimental reports have demonstrated that the warpage of PCBs can also be significantly influenced by these other Cu patterns [16, 17]. Furthermore, to the best of the author's knowledge, a warpage simulation technique that simultaneously includes the anisotropic and viscoelastic properties of PCB materials has yet to have been reported; it was generally believed that this procedure would require huge computing times and effort. However, the anisotropic viscoelastic properties of PCB layers should be accounted for in order to obtain accurate warpage simulation because most of the materials composing the PCB structure (BT-core and SR) have different viscoelastic properties with respect to their material orientations. Viscoelasticity is a very important parameter to consider in order to accurately predict PCB warpage because time is a representative variable in the manufacturing process of PCBs (e.g. the temperature changing ratio, delay time, number of reflow cycles, etc).

In this study, the warpage simulation of multi-layer PCBs was conducted as a function of various Cu patterns and their viscoelastic properties. The thermo-mechanical properties of the Cu patterns in the PCBs were obtained from virtual test simulations and homogenized with an anisotropic viscoelastic composite shell model. To define the anisotropic viscoelastic properties of the unit patterns, a user-defined composite shell subroutine (UGENS) was developed. Viscoelastic analysis of the PCB during the reflow process was performed by using ABAQUS combined with the user-defined composite shell subroutine that was developed. Additionally, the warpage of PCBs during the reflow process was measured experimentally using shadow moiré. These results were compared with those from the simulation in order to verify the developed analysis technique.

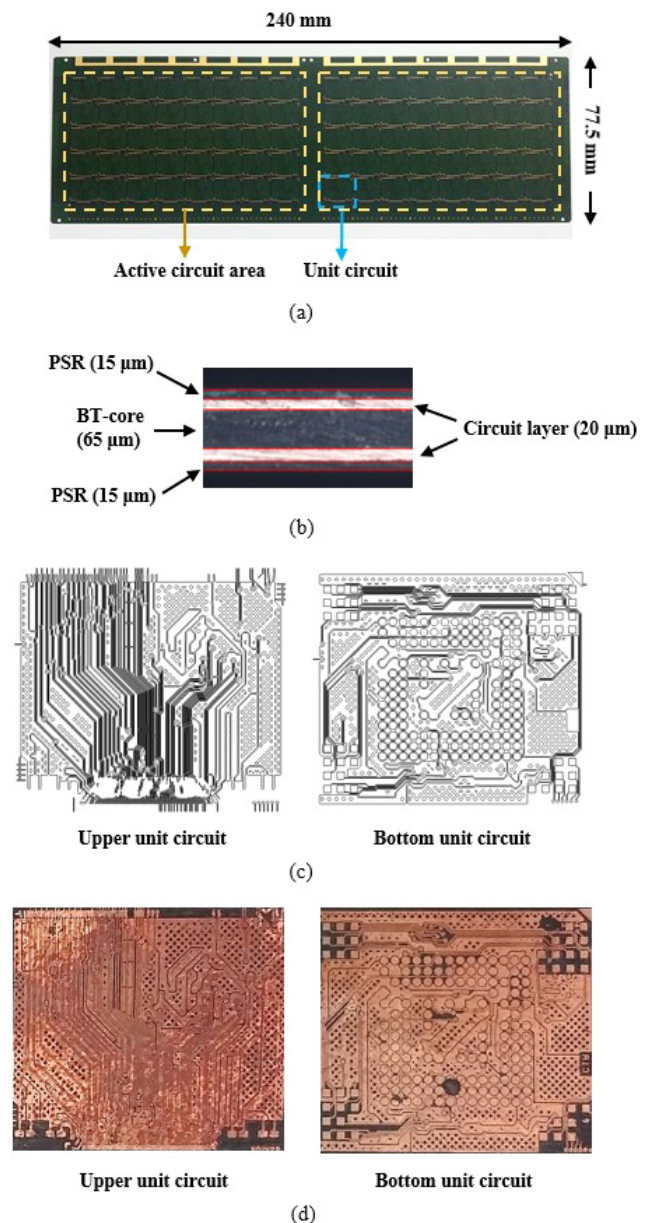


Figure 1. Multi-layer PCB substrate: (a) top view of entire PCB; (b) microscopic image of PCB cross-section; (c) drawing of unit copper circuit; (d) microscopic image of unit copper circuit on BT core.

2. Warpage simulation of a multi-layer PCB

The picture and layer information of the multi-layer PCB used in this study are shown in figure 1. The PCB is composed of one woven glass fabric/bismaleimide triazine epoxy composite (BT-core) layer, double copper (Cu) circuit layers, and photoimageable solder resist (PSR) layers that cover the top and bottom of the Cu layers. The thicknesses of the BT-core, Cu layers, and PSR layer are $65\ \mu\text{m}$, $20\ \mu\text{m}$, and $15\ \mu\text{m}$, respectively. The Cu layers have two large active circuit areas that consist of 40 unit circuits each (figure 1(a)). The upper and bottom Cu layers consist of several different Cu circuit shapes with a variety of patterns, such as dummy, line trace, circular, and square pads, as shown in figure 1(c). With the exception of the active circuit area, the grid shape of the Cu

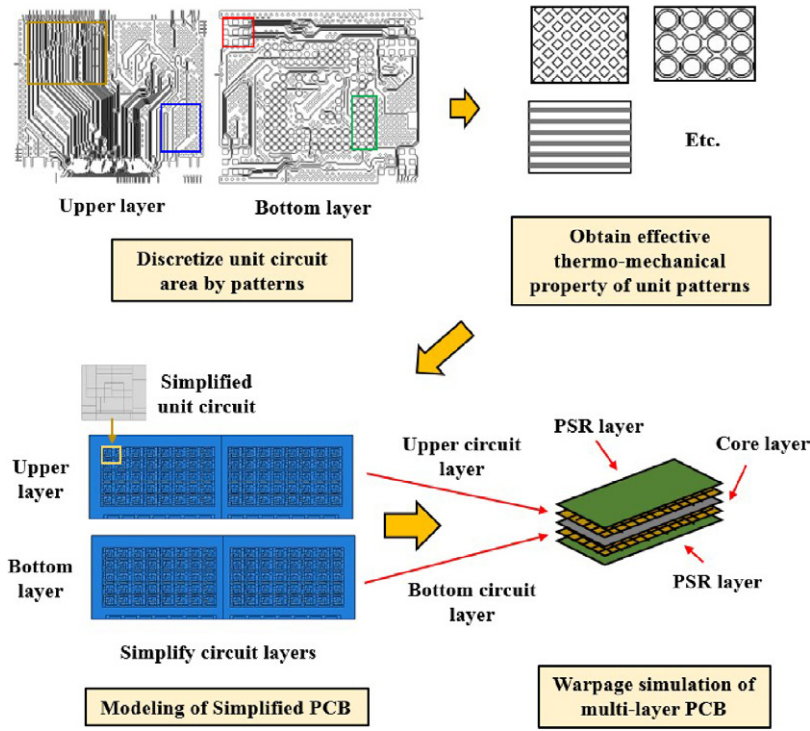


Figure 2. Schematic diagram of steps for PCB warpage simulation.

patterns filled the remaining areas. The multi-layer PCB and circuit information were provided by SAMSUNG Electronics. Detailed information about the Cu patterns is described in section 2.1.

Because the circuit of the PCB used in this study is too complicated (a total of 80 unit circuits) to model all of the circuits individually, we devised a homogenized pattern modeling technique by using the effective thermo-mechanical properties. Figure 2 shows each of the steps for the warpage simulation of the PCB using the developed pattern modeling method. First, the unit circuit area of each Cu layer was discretized based on the shape of the patterns. Then, the effective thermo-mechanical properties of each unit pattern were obtained for the homogenized pattern models. Finally, the entire PCB was modeled using the simplified unit circuit model, and the warpage simulation was performed under the reflow condition. The details of these simulation procedures are described in section 2.2.

2.1. Effective thermo-mechanical properties of PCB patterns

Figure 3 shows the finite element analysis (FEA) models of the Cu unit patterns. The whole PCB area (the upper and bottom active circuits and grid area) can be represented by a combination of these patterns. The geometric properties of the Cu patterns were based on the drawings of the PCB provided by SAMSUNG Electronics. All of the unit pattern models were composed of Cu and PSRs. Thus, the effective viscoelastic response of the unit patterns, which consist of the elastic Cu and the viscoelastic PSR, can be modeled as the matrix relaxation moduli of the PSR/Cu pattern composite. In this work, the viscoelastic properties of

the PSR and BT-core were modeled by using a Prony series to represent the time and temperature dependent mechanical properties. The relaxation modulus of PSRs is represented by the Prony series as:

$$E(t) = E_{\infty} + \sum_{i=1}^n E_i e^{-t/\rho_i}, \tag{1}$$

where t is time, E_{∞} is the long-term modulus, E_i are the Prony coefficients, and ρ_i are the relaxation times. Also, the time-temperature shift factor is expressed in terms of the Williams–Landel–Ferry (WLF) equation as:

$$\log a_T = -\frac{c_1(T - T_0)}{c_2 + (T - T_0)}, \tag{2}$$

where c_1 and c_2 are material constants depending on the particular material and the logarithm is base ten. T_0 is the reference temperature and a_T is the shift factor, which expresses the ratio of relaxation times between the reference temperature and the specific temperature T as:

$$a_T = \frac{\rho(T)}{\rho(T_0)}, \tag{3}$$

where ρ is the relaxation time. The viscoelastic properties of the PSR and BT-core can be obtained through a series of vibration tests (performed for the same materials by Joo *et al*) [18]. The parameters of the Prony series and relaxation master curve of the PCB materials are represented in table 1 and figure 4(a), respectively. The temperature dependent coefficients of thermal expansion (CTEs) for the PCB materials were provided by SAMSUNG Electronics, as shown in figure 4(b).

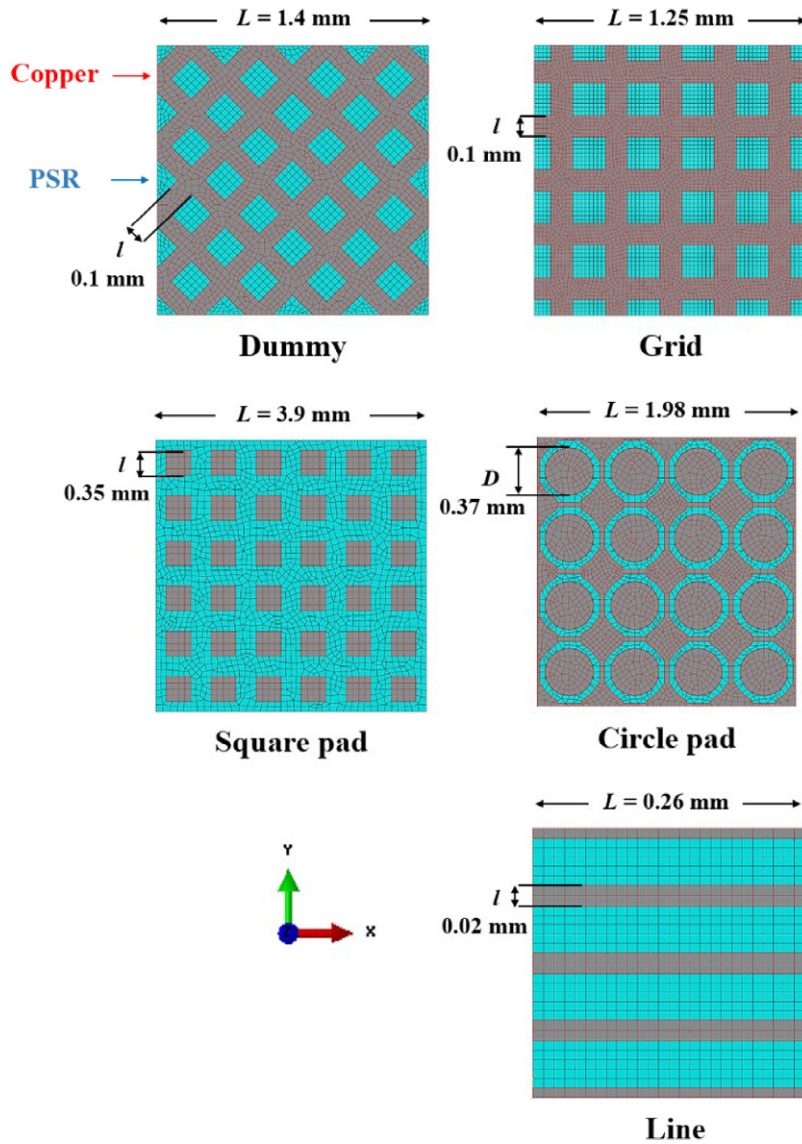


Figure 3. Finite element models for measuring effective thermo-mechanical property of unit patterns.

Table 1. Relaxation times and relaxation coefficients of PCB materials.

i	ρ_i	BT-core	PSR	Copper
		E_i (GPa)		
∞	—	18.30	0.02	65.44
1	1.0×10^{-6}	2.25×10^{-3}	1.00×10^{-1}	—
2	1.0×10^{-5}	1.40×10^{-14}	1.18×10^{-1}	—
3	1.0×10^{-4}	2.72×10^{-5}	1.18×10^{-1}	—
4	1.0×10^{-3}	8.20×10^{-6}	1.15×10^{-1}	—
5	1.0×10^{-1}	2.98×10^{-1}	1.00×10^{-1}	—
6	1.0×10^1	1.38	7.84×10^{-2}	—
7	1.0×10^3	2.08	2.76×10^{-2}	—
WLF constants	T_0 (K)	333	333	
	C_1	18.54	20.56	
	C_2	200.64	202.83	

The viscoelastic properties of the Cu patterns were determined directly from the constituent properties by FEA of the unit cell. This approach was adopted from the report of Brinson and Knauss [19], which calculated the

effective viscoelastic properties of a unidirectional fiber composite. In the case of an anisotropic line pattern, the constitutive relationships for the homogenized shell are described as:

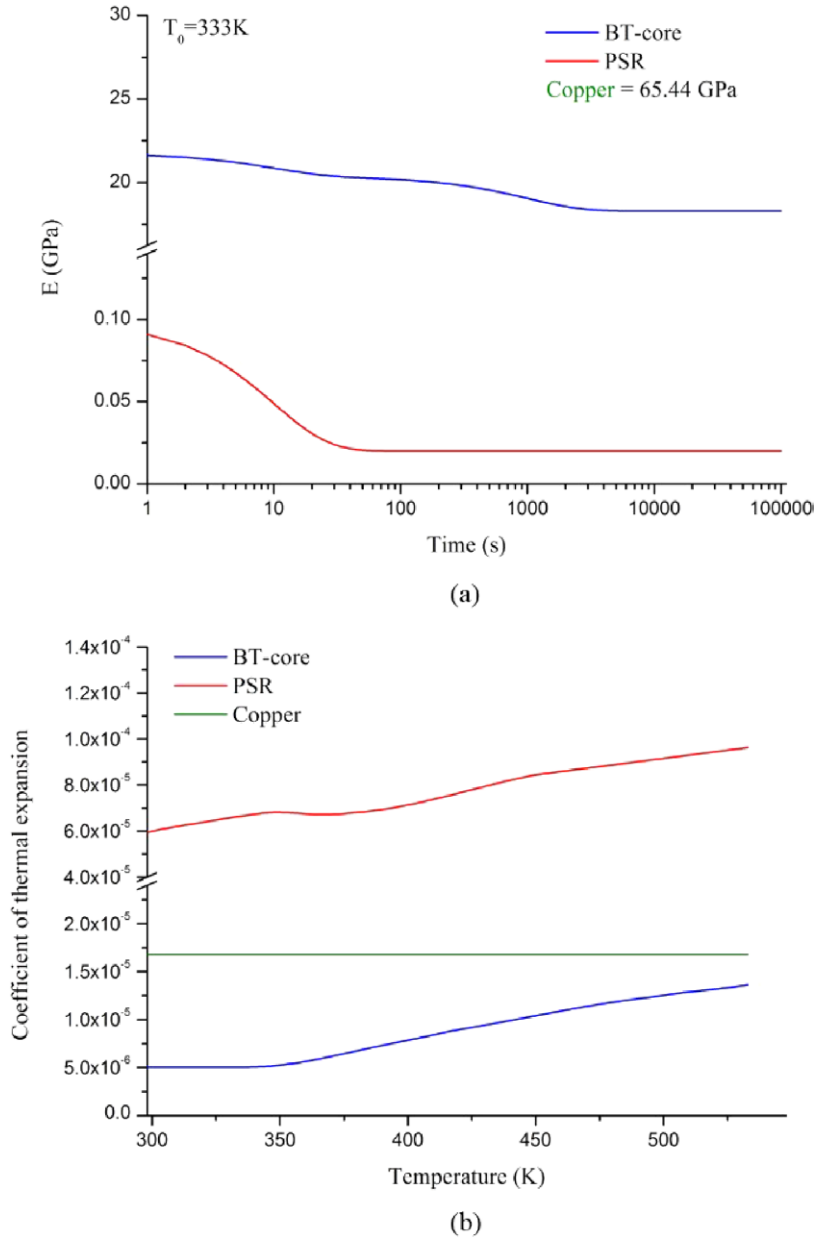


Figure 4. Mechanical properties of PCB materials: (a) viscoelastic master curves at a reference temperature of $T_0 = 333$ K; (b) temperature dependent CTEs.

$$\begin{aligned}
 [N(t)] &= \int_0^t ([A(t-s)][\dot{\varepsilon}(s)] + [B(t-s)][\dot{\kappa}(s)])ds \\
 [M(t)] &= \int_0^t ([B(t-s)][\dot{\varepsilon}(s)] + [D(t-s)][\dot{\kappa}(s)])ds,
 \end{aligned} \tag{4}$$

$$ABD(t) = \begin{bmatrix} A_{11}(t) & A_{12}(t) & A_{16}(t) & B_{11}(t) & B_{12}(t) & B_{16}(t) \\ A_{21}(t) & A_{22}(t) & A_{26}(t) & B_{21}(t) & B_{22}(t) & B_{26}(t) \\ A_{61}(t) & A_{62}(t) & A_{66}(t) & B_{61}(t) & B_{62}(t) & B_{66}(t) \\ B_{11}(t) & B_{12}(t) & B_{16}(t) & D_{11}(t) & D_{12}(t) & D_{16}(t) \\ B_{21}(t) & B_{22}(t) & B_{26}(t) & D_{21}(t) & D_{22}(t) & D_{26}(t) \\ B_{61}(t) & B_{62}(t) & B_{66}(t) & D_{61}(t) & D_{62}(t) & D_{66}(t) \end{bmatrix}. \tag{5}$$

where the matrix $[N]$ is the force, $[M]$ is the moment, and $[\varepsilon]$ and $[\kappa]$ denote the mid-plane strains and out-of-plane curvatures, respectively. The matrices $[A]$, $[B]$, and $[D]$ represent the in-plane stiffness, stretching–bending coupling, and bending stiffness matrices, respectively, which have been generally used in composite shell modeling in classical laminate theory [20]. They are combined to give the ABD stiffness matrix as follows:

Because the homogenized shell is symmetric about its mid-plane, the bending–stretching coupling matrix $[B]$ is zero. A_{16} and A_{26} also become zero due to the decoupling between stretching and shearing. Similarly, bending and twisting are decoupled as $D_{16} = D_{26} = 0$. Then, equation (5) can be written as [20]:

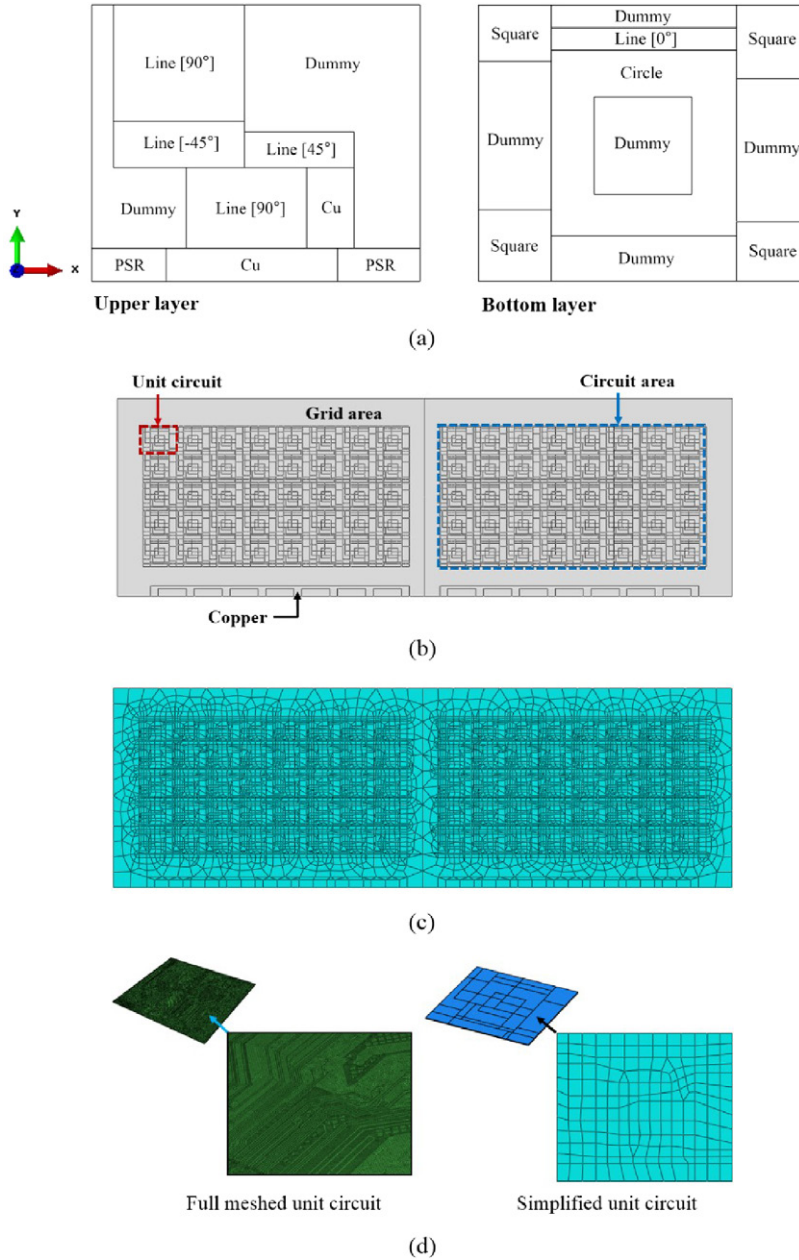


Figure 5. Finite element model of simplified entire PCB: (a) Discretized unit circuit area; (b) simplified model of PCB circuit layer; (c) meshed PCB layer for warpage simulation; (d) comparison of meshed element.

$$ABD(t) = \begin{bmatrix} A_{11}(t) & A_{12}(t) & 0 & 0 & 0 & 0 \\ A_{21}(t) & A_{22}(t) & 0 & 0 & 0 & 0 \\ 0 & 0 & A_{66}(t) & 0 & 0 & 0 \\ 0 & 0 & 0 & D_{11}(t) & D_{12}(t) & 0 \\ 0 & 0 & 0 & D_{21}(t) & D_{22}(t) & 0 \\ 0 & 0 & 0 & 0 & 0 & D_{66}(t) \end{bmatrix}. \quad (6)$$

In this work, three virtual tests were needed for the x -, y -, and xy -directions, respectively, in order to acquire the independent time-varying functions in $ABD(t)$. The virtual relaxation tests were performed by stretching each edge to a strain of 0.005 over 1 s and then holding for 10^5 s. For all of these analyses, the periodic displacement boundary conditions

were enforced between each pair of opposite boundary edges of the unit cells. The CTEs of each material were accounted for in order to remove the effects of expansion caused by the temperature. The temperature was set to 333 K, which is the reference temperature of the PSR under the WLF constants (see table 1). Because Cu has only elastic properties, the viscoelastic master curve of the unit patterns can be obtained directly at this temperature and the WLF constants are the same as the pure PSR. Similarly, each entry in the $ABD(t)$ matrix was modeled with the same relaxation times as the matrix (the PSR in this study) [21].

Then, the reduced stiffness matrix $[Q(t)]$ can be calculated from the results of the stress relaxation tests ($E_x(t)$, $E_y(t)$, and $G_{xy}(t)$) as follows:

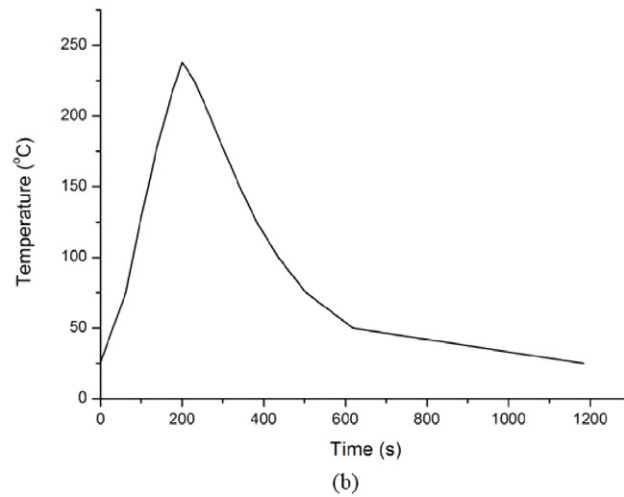
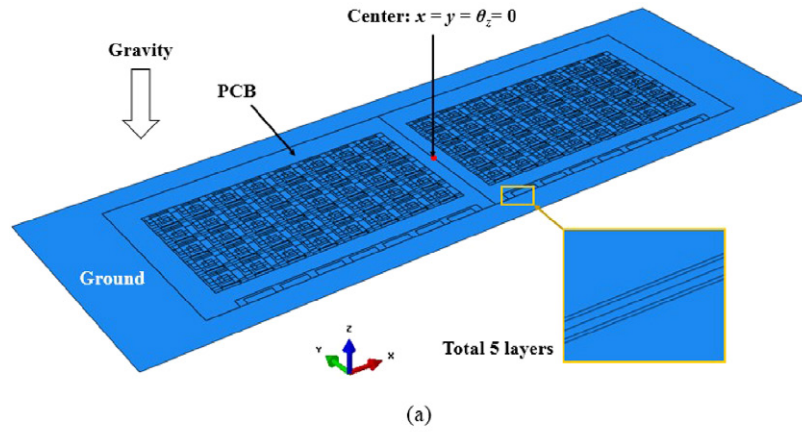


Figure 6. Finite element model of entire PCB for warpage simulation: (a) assembled FEA model and boundary condition; (b) temperature history from reflow experiment.

$$[Q(t)] = \begin{bmatrix} \frac{E_x(t)}{1 - \nu_{12}\nu_{21}} & \frac{\nu_{12}E_y(t)}{1 - \nu_{12}\nu_{21}} & 0 \\ \frac{\nu_{12}E_y(t)}{1 - \nu_{12}\nu_{21}} & \frac{E_y(t)}{1 - \nu_{12}\nu_{21}} & 0 \\ 0 & 0 & G_{xy}(t) \end{bmatrix}, \quad (7)$$

where ν_{12} and ν_{21} are the major and minor Poisson’s ratio of the unit pattern obtained from the virtual relaxation tests. In this work, Poisson’s ratios were assumed to be constant values to simplify the calculation. The bending behavior of the unit shells is primarily 1D; thus, the effect of Poisson’s ratio is expected to be minor [22]. Based on the result of $[Q(t)]$, the corresponding constituents of $[A(t)]$ and $[D(t)]$ can be obtained using the following equations [20]:

$$\begin{aligned} [A(t)] &= [Q(t)] \times t \\ [D(t)] &= [Q(t)] \times \frac{t^3}{12}, \end{aligned} \quad (8)$$

where t is the thickness of the unit pattern. From these results, the Prony coefficients of each of the constituents of $ABD(t)$ were determined by numerical fitting with respect to time.

For the other patterns (dummy, grid, circle, and square pad), the viscoelastic properties were homogenized with the isotropic shell because they have the same Cu shapes repeated

in both the x -direction and y -direction; thus, the anisotropic effects were negligible (see figure 3). For these patterns, the viscoelastic properties were determined by the representative virtual relaxation test for only the x -direction.

Also, the CTE of each unit pattern was obtained by virtual thermal expansion tests. In this work, a temperature change from 298 to 450 K was applied to the FEA model of the unit pattern (as opposed to using strain constraints). To remove the viscoelastic effects during simulation, only the CTE and elastic properties of the PSR and Cu were included in the model. Similar to the determination of the viscoelastic properties, simulations were performed in the x - and y -directions (for the line pattern) and in only the x -direction (for the other patterns).

2.2. Finite element analysis of the simplified PCB model

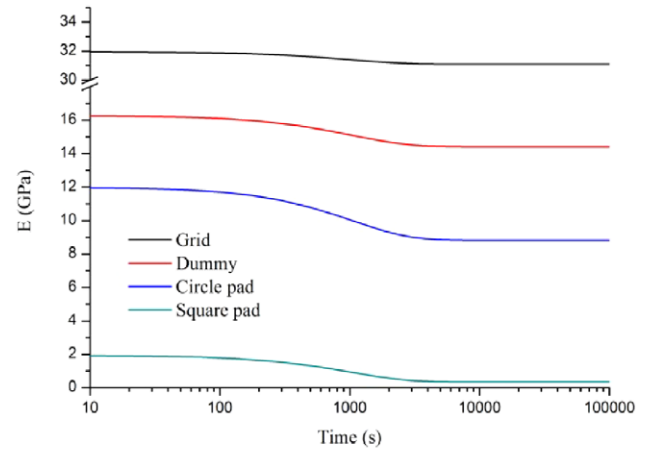
Figure 5(a) shows the simply discretized unit circuit area based on the shape of the Cu patterns (figure 3). In the case of the line pattern, the material orientation must be accounted for (due to the anisotropic viscoelastic properties). By using this model, the entire PCB circuit layer could be modeled simply, as shown in figure 5(b). The thermo-mechanical properties of the Cu patterns obtained from section 2.1 were applied to each of the areas. In the case of the line pattern, the viscoelastic



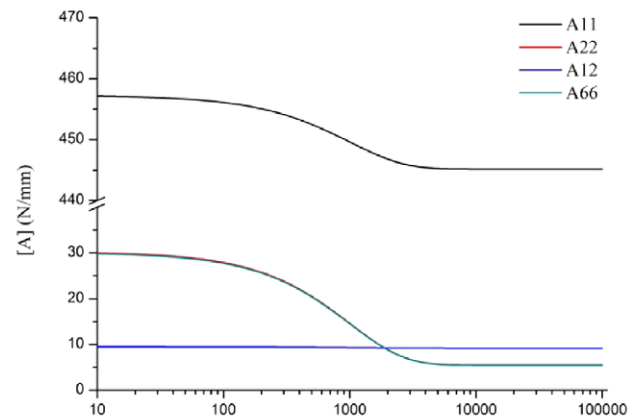
Figure 7. Experimental setup of shadow moiré for PCB warpage measuring.

stiffness properties were defined by assigning the $ABD(t)$ matrix via the user-defined shell section subroutine (UGENS) with the material orientation. Figure 5(c) shows the meshed PCB circuit layer with 9421 reduced integration quadrilateral shell elements (S4R). The other layers were also meshed in the same manner to the circuit layer to ensure stability of convergence and to save simulation time. As shown in figure 5(d), it is noteworthy that almost 95 000 meshes were needed to model just the upper unit circuit when using the conventional modeling technique (which exactly accounts for all of the Cu circuits). Furthermore, using the conventional modeling technique, viscoelastic analysis is almost impossible due to the huge computation size and the data storage requirements of the simulation. Conversely, the homogenized anisotropic viscoelastic composite shell modeling technique developed in this study can reduce the number of meshes and computation time dramatically.

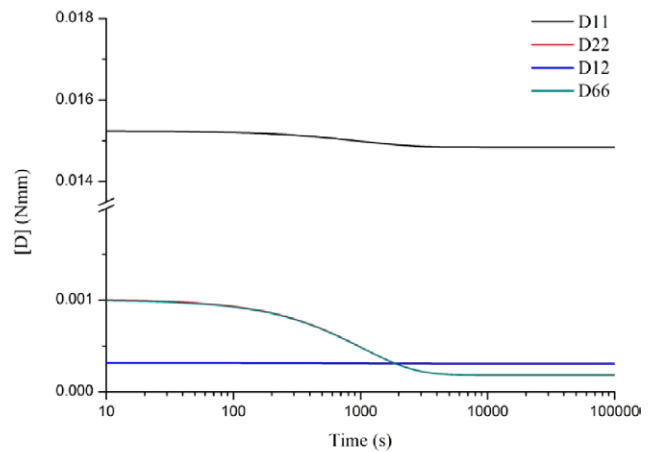
The final FEA model for the warpage simulation of the PCB is shown in figure 6(a). A total of five layers were assembled on the rigid ground and a gravity load was applied during all of the simulation steps. The gaps between each of the layers were determined based on their thicknesses, and the interfaces between each of the layers were constrained to have perfect bonding by using the *TIE function in ABAQUS. Also, a frictionless contact interaction was enforced between the bottom PSR layer and the ground through the *SURFACE INTERACTION command. Additionally, movements in the



(a)



(b)



(c)

Figure 8. Viscoelastic stiffness of unit patterns obtained from stress relaxation simulation (333 K): (a) isotropic patterns; (b) in-plane stiffness of line pattern; (c) bending stiffness of line pattern.

x- and y-directions and the rotational freedom for the z-direction of the center node in the BT-core layer were constricted. Then, quasi-static analyses were carried out by using the *VISCO step of ABAQUS with the reflow temperature, as shown in figure 6(b). This was measured from the warpage experiment in the shadow moiré, as shown in figure 7; this will be described in detail in section 3. The warpage simulation was also performed using only the elastic properties of

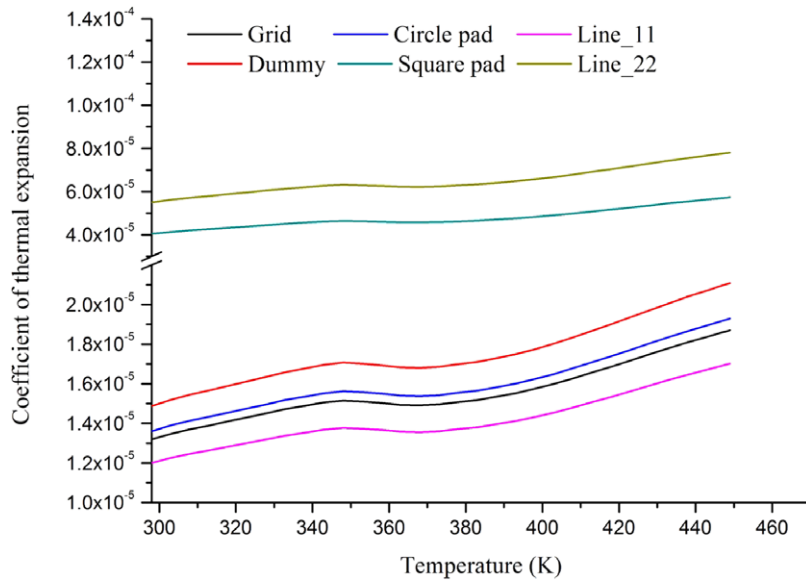


Figure 9. Temperature dependent CTE of unit patterns obtained from simulation.

Table 2. Relaxation times and relaxation coefficients of copper patterns.

<i>i</i>	ρ_i	Grid	Dummy	Circle pad	Square pad
		E_i (GPa)			
∞	—	31.09	14.42	8.83	0.35
1	1.0×10^{-6}	6.46×10^{-17}	8.44×10^{-9}	8.00×10^{-4}	2.12×10^{-8}
2	1.0×10^{-5}	3.54×10^{-16}	8.00×10^{-14}	2.98×10^{-4}	3.25×10^{-11}
3	1.0×10^{-4}	5.00×10^{-11}	1.59×10^{-18}	4.29×10^{-6}	3.44×10^{-6}
4	1.0×10^{-3}	5.11×10^{-5}	1.00×10^{-10}	1.24×10^{-6}	1.07×10^{-2}
5	1.0×10^{-1}	2.09×10^{-2}	4.16×10^{-2}	7.41×10^{-2}	2.70×10^{-2}
6	1.0×10^1	6.62×10^{-3}	9.70×10^{-3}	1.13×10^{-3}	1.16×10^{-2}
7	1.0×10^3	8.64×10^{-1}	1.86	3.18	1.59

Table 3. Relaxation times and relaxation coefficients of line pattern.

<i>i</i>	ρ_i	A11	A22	A12	A66
		E_i (GPa)			
∞	—	445.18	5.522	9.236	5.487
1	1.0×10^{-6}	0.0588	0.0983	0.0012	0.098
2	1.0×10^{-5}	0.0577	1.928	0.0048	0.392
3	1.0×10^{-4}	0.173	1.158×10^{-10}	1.199×10^{-15}	6.794×10^{-10}
4	1.0×10^{-3}	1.340×10^{-11}	9.831×10^{-14}	3.163×10^{-14}	1.039×10^{-10}
5	1.0×10^{-1}	6.118×10^{-9}	1.427×10^{-14}	1.358×10^{-14}	1.038×10^{-10}
6	1.0×10^1	5.982×10^{-13}	0.00176	1.032×10^{-13}	1.416×10^{-15}
7	1.0×10^3	12.08	24.752	0.251	24.594
∞	—	D11	D22	D12	D66
1	1.0×10^{-6}	0.01484	1.841×10^{-4}	3.079×10^{-4}	1.829×10^{-4}
2	1.0×10^{-5}	1.935×10^{-6}	3.262×10^{-18}	3.768×10^{-8}	3.258×10^{-6}
3	1.0×10^{-4}	7.739×10^{-6}	7.744×10^{-19}	7.280×10^{-7}	0.650
4	1.0×10^{-3}	2.305×10^{-15}	8.415×10^{-4}	2.580×10^{-15}	6.302×10^{-14}
5	1.0×10^{-1}	3.454×10^{-17}	3.262×10^{-14}	1.785×10^{-19}	5.941×10^{-16}
6	1.0×10^1	1.966×10^{-18}	3.262×10^{-14}	3.839×10^{-19}	7.037×10^{-14}
7	1.0×10^3	4.590×10^{-19}	6.846×10^{-19}	4.906×10^{-18}	3.801×10^{-15}
		4.033×10^{-4}	8.087×10^{-4}	8.347×10^{-6}	8.198×10^{-4}

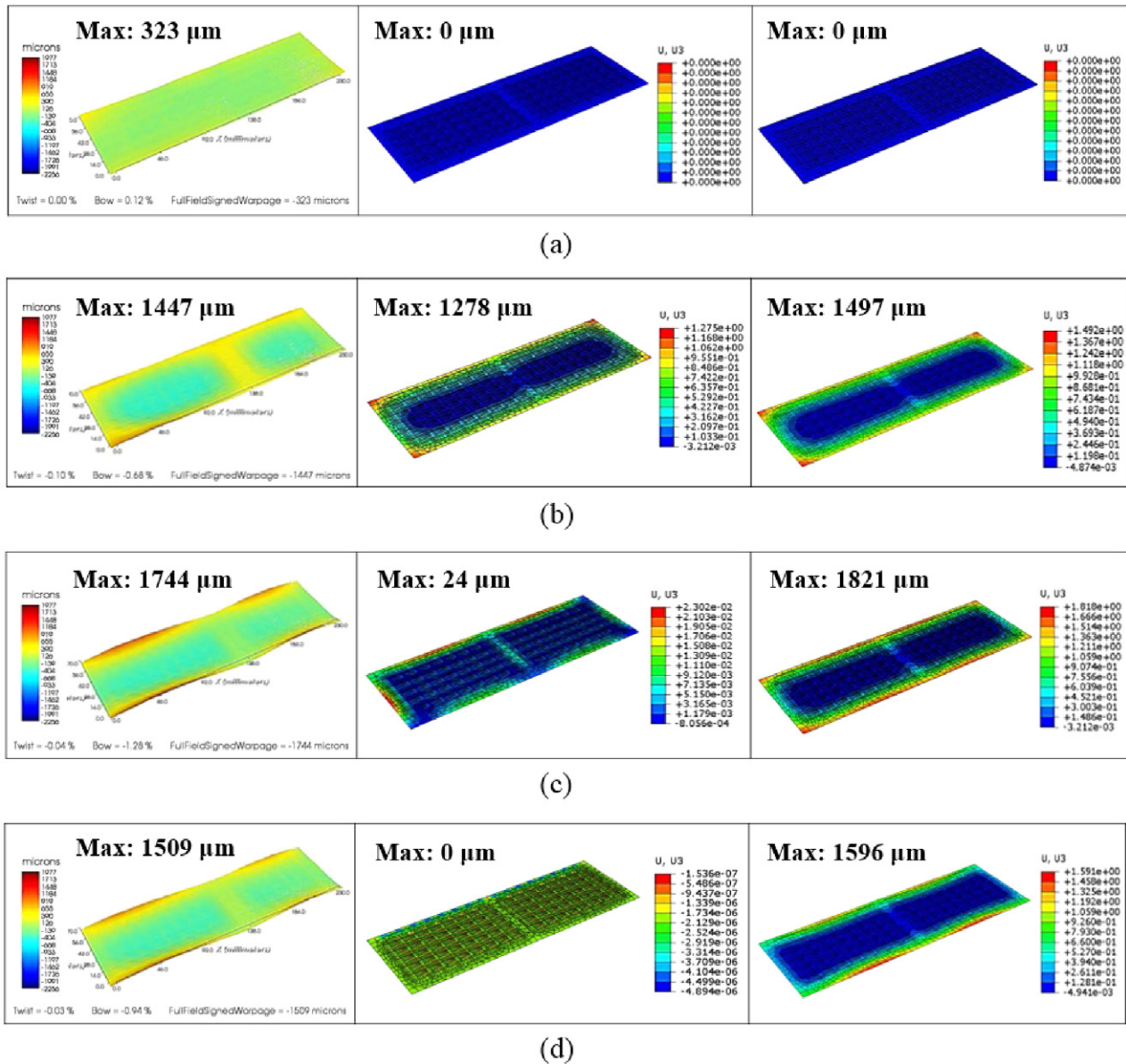


Figure 10. PCB warpage result from experiment and simulation (left: experiment, mid: elastic simulation, right: viscoelastic simulation): (a) initial state (25 °C); (b) at maximum temperature (238 °C); (c) decent of temperature (50 °C); (d) end of reflow (25 °C).

the PCB materials for comparison with the simulation results from the viscoelastic warpage simulation developed in this study.

3. Experimental verification

In this work, the warpage of a multi-layer PCB during the reflow process was measured by the shadow moiré test. The shadow moiré technique measures the topography of the surface and its deviation from a planar surface [23]. Figure 7 shows the shadow moiré equipment (TherMoiré AXP, Akrometrix, USA) and the PCB specimen, which is sprayed to be white for exact warpage results. For the warpage measuring, 100 line-per-inch (LPI) of the reference grating line density was used. The reflow temperature history of the specimen during warpage testing was monitored by a K-type thermo-couple (located on the PCB specimen) with a continuous detection

system with a precision of ± 1 °C. This information was applied to the warpage simulations (figure 6(b)).

4. Result and discussion

4.1. Thermo-mechanical properties of unit patterns

Figure 8(a) shows the homogenized viscoelastic master curves of the Cu unit patterns obtained from the virtual relaxation tests at a reference temperature of 333 K. It can be found that the moduli of all unit patterns decreased with time. In particular, the square pad showed a much smaller modulus compared to the other patterns. This was caused by the fact that all of the Cu pads in its unit pattern were isolated by the PSR matrix (figure 3). After 10000 s, the viscoelastic modulus of the square pad was decreased to almost zero, which is similar to the modulus of the pure PSR.

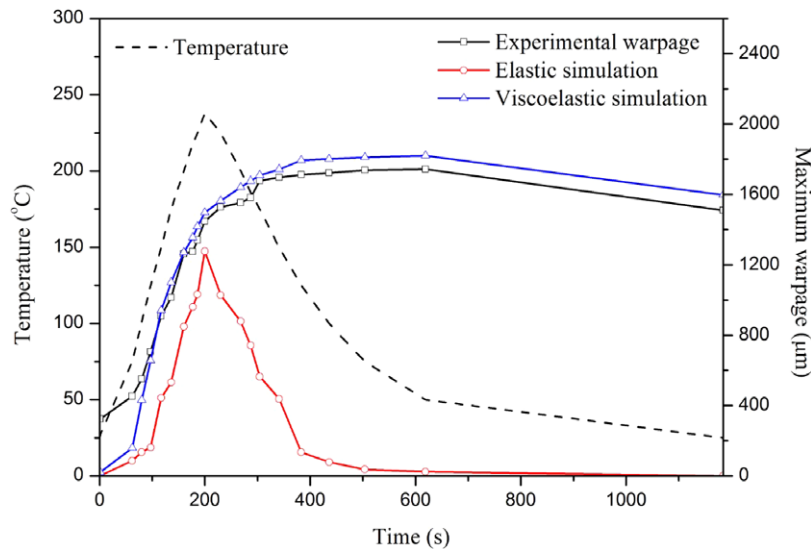


Figure 11. Results comparison of maximum warpage of PCB during reflow process.

In the case of the anisotropic line pattern, the viscoelastic master curves were plotted by each of the constituents of $ABD(t)$, as shown in figures 8(b) and (c). It is noteworthy that a large difference was found with respect to the direction of the stiffness for both the in-plane stiffness (A11 and A22) and the bending stiffness (D11 and D22). This was also caused by the fact that the Cu shapes in the unit line pattern were isolated by the PSR matrix in the y -direction. From these results, it can be concluded that anisotropic homogenization should be performed according to the shape of the Cu patterns to ensure accurate prediction of the Cu pattern behavior. Also, the 12 and 66 moduli showed significantly smaller values compared to the 11 direction in both the in-plane stiffness and the bending stiffness. This is caused by the fact that the stiffness in the 12 and 66 direction of the line pattern are significantly affected by the PSR properties (but not by the Cu).

The CTEs of the unit patterns obtained from the virtual expansion tests can be seen in figure 9. Similar to the viscoelastic stiffness, the CTE of the square pad and the y -direction of the line pattern showed much higher values (similar to the pure PSR) compared to the values of the other patterns. This was also caused by the fact that the Cu shapes in their unit patterns were isolated by the PSR matrix. Based on these results, it can be concluded that the thermo-mechanical properties of the Cu isolated unit pattern are mostly affected by the properties of PSR rather than those of the Cu.

Finally, the thermo-mechanical properties of the PCB patterns can be defined by using the Prony coefficients (tables 2 and 3) with the temperature dependent CTE. In the case of the line pattern, the Prony coefficients of each of the constituents were input by the user-defined shell section subroutine (UGENS).

4.2. Warpage of the multi-layer PCB

Figure 10 shows the warpage of the PCB during the reflow process that was obtained from the shadow moiré experiment and the simulation using the elastic and viscoelastic properties

of the PCB materials, respectively. From the experimental results, it was found that significant warpage was generated at both sides of the edges (with a maximum value of $1744 \mu\text{m}$). Also, a large amount of residual warpage ($1509 \mu\text{m}$) remained, despite the fact that the reflow process was completed (see the left line figure in figure 10(d)). This is an important piece of information regarding for the real reflow process because the remaining residual warpage can be a significant problem during additional manufacturing processes (e.g. mismatching from the mounted microelectronic packages, disconnection of solder paste bridging, or crack generation of solder joints). However, in the case of elastic warpage simulation, there was no remaining residual warpage after the reflow process, although similar warpage was found at the maximum temperature compared to the experimental results (see the middle line figures in figures 10 and 11). Most of the warpage was removed as the temperature decreased, and it completely disappeared after the reflow with the exception of slight warpage caused by the gravity load, which is expected (the middle line figures in figures 10(d) and 11).

The results of the warpage simulation using the developed viscoelastic model and the maximum warpage values are represented in figures 10 and 11, respectively. It was found that the simulation results showed good agreement with the warpage values and positions for each temperature point when compared to the experimental result. Especially, it was found that large amounts of residual warpage remained at $50 \text{ }^\circ\text{C}$ in the experiment and simulation ($1509 \mu\text{m}$ and $1596 \mu\text{m}$, respectively) after the reflow process (figures 10(c) and 11). This was caused by the fact that the difference in the thermo-mechanical properties between each layer increased with respect to the time and temperature history (due to the viscoelastic properties). Additionally, the remaining warpage at $25 \text{ }^\circ\text{C}$, after the reflow process, could be also be predicted accurately by using the developed anisotropic viscoelastic warpage simulation (figures 10(d) and 11). Based on these results, it can be concluded that both the maximum warpage and the remaining residual warpage of multi-layer PCBs after

the reflow process can be accurately predicted by using the viscoelastic warpage simulation technique developed in this study.

5. Conclusion

In this study, the warpage simulation of a multi-layer PCB was performed as a function of various copper patterns and their viscoelastic properties. The homogenized isotropic and anisotropic thermo-mechanical properties of the unit patterns could be obtained from the virtual relaxation and thermal expansion tests. Finally, the warpage of the PCB during the reflow process was predicted by using a simplified PCB model with the developed viscoelastic warpage simulation technique. From these results, we concluded that both the maximum warpage and the remaining warpage of multi-layer PCBs can be accurately predicted by using the developed viscoelastic warpage simulation. It is expected that the simulation technique established in this study can be widely used to predict warpage in various multi-layer PCB products.

Acknowledgments

This work was supported by SAMSUNG Electronics (No 201300000000305) and the National Research Foundation of Korea (NRF) funded by the Ministry of Education (No 2012R1A6A1029029 and No 2013M2A2A9043280). Also, this work was supported by the Technology Innovation Program (or Industrial Strategic technology development program, 10048913, Development of the cheap nano-ink which is sintered in the air for smart devices) funded By the Ministry of Trade, Industry and Energy (MI, Korea).

References

- [1] Tummala R R 2001 *Fundamentals of Microsystems Packaging* (New York: McGraw-Hill)
- [2] Gupta A, Barron L, Brainin M and Lee J-B 2014 Reduction of out-of-plane warpage in surface micromachined beams using corrugation *J. Micromech. Microeng.* **24** 065023
- [3] O'Mahony C, Olszewski O, Hill R, Houlihan R, Ryan C, Rodgers K, Kelleher C, Duane R and Hill M 2014 Reliability assessment of MEMS switches for space applications: laboratory and launch testing *J. Micromech. Microeng.* **24** 125009
- [4] Tian Y, Wang C and Liu D 2002 Thermalmechanical behavior of PBGA package during laser and hot air reflow soldering. *Proc. 4th IEEE Int. Symp. on Electronic Materials and Packaging, 2002* pp 293–9
- [5] Hassell P B 2001 Advanced warpage characterization: location and type of displacement can be equally as important as magnitude *Proc. of Pan Pacific Microelectronics Symposium Conf.* pp 163–9
- [6] Aleck B 1949 Thermal stresses in a rectangular plate clamped along an edge *Trans. ASME, J. Appl. Mech.* **16** 118–22
- [7] Lee M and Jasiuk I 1991 Asymptotic expansions for the thermal stresses in bonded semi-infinite bimaterial strips *J. Electron. Packag.* **113** 173–7
- [8] Timoshenko S 1925 Analysis of bi-metal thermostats *J. Opt. Soc. Am.* **11** 233–55
- [9] Wang Y, Low K, Che F, Pang H and Yeo S 2003 Modeling and simulation of printed circuit board drop test *5th IEEE Conf. on Electronics Packaging Technology (EPTC 2003)* pp 263–8
- [10] Wu J, Zhang R R, Radons S, Long X and Stevens K K 2002 Vibration analysis of medical devices with a calibrated FEA model *Comput. Struct.* **80** 1081–6
- [11] Yang Q, Pang H, Wang Z, Lim G, Yap F and Lin R 2000 Vibration reliability characterization of PBGA assemblies *Microelectron. Reliab.* **40** 1097–107
- [12] Lau J H, Wong C, Prince J L and Nakayama W 1998 *Electronic Packaging: Design, Materials, Process, and Reliability* (New York: McGraw-Hill)
- [13] Lee M 2000 Finite element modelling of printed circuit boards (PCBs) for structural analysis *Circuit World* **26** 24–9
- [14] Moore T D and Jarvis J L 2002 The effects of in-plane orthotropic properties in a multi-chip ball grid array assembly *Microelectron. Reliab.* **42** 943–9
- [15] Wang Y, Low K, Pang H, Hoon K H, Che F and Yong Y 2006 Modeling and simulation for a drop-impact analysis of multi-layered printed circuit boards *Microelectron. Reliab.* **46** 558–73
- [16] Grenestedt J L and Hutapea P 2002 Using waviness to reduce thermal warpage in printed circuit boards *Appl. Phys. Lett.* **81** 4079–81
- [17] Hutapea P, Grenestedt J L, Modi M, Mello M and Frutschy K 2006 Prediction of microelectronic substrate warpage using homogenized finite element models *Microelectron. Eng.* **83** 557–69
- [18] Joo S-J, Park B, Kim D-H, Kwak D-O, Song I-S, Park J and Kim H-S 2015 Investigation of multilayer printed circuit board (PCB) film warpage using viscoelastic properties measured by a vibration test *J. Micromech. Microeng.* **25** 035021
- [19] Brinson L and Knauss W 1992 Finite element analysis of multiphase viscoelastic solids *J. Appl. Mech.* **59** 730–7
- [20] Lee D G and Suh N P 2005 Axiomatic design and fabrication of composite structures-applications in robots, machine tools, and automobiles *Axiomatic Design and Fabrication of Composite Structures-Applications in Robots, Machine Tools, and Automobiles* ed D G Lee and N P Suh (Foreword by Dai Gil Lee and Nam Pyo Suh) (Oxford: Oxford University Press) p 732 November 2005. ISBN-10: 0195178777. ISBN-13: 9780195178777 1
- [21] Kwok K and Pellegrino S 2012 Micromechanical modeling of deployment and shape recovery of thin-walled viscoelastic composite space structures *53rd AIAA/ASME/ASCE/AHS/ASC Structures, Structural Dynamics and Materials Conf. 20th AIAA/ASME/AHS Adaptive Structures Conf. 14th AIAA*
- [22] Hilton H H 2001 Implications and constraints of time-independent Poisson ratios in linear isotropic and anisotropic viscoelasticity *J. Elast. Phys. Sci. Solids* **63** 221–51
- [23] Stiteler M R and Ume I 1997 System for real-time measurement of thermally induced PWB/PWA warpage *Trans. ASME, J. Electron. Packag.* **119** 1–7