

Warpage Simulation of a Multilayer Printed Circuit Board and Microelectronic Package Using the Anisotropic Viscoelastic Shell Modeling Technique That Considers the Initial Warpage

Do-Hyoung Kim, Sung-Jun Joo, Dong-Ok Kwak, and Hak-Sung Kim

Abstract—In this paper, the warpage simulation of a high-density multilayer printed circuit board (PCB) for solid-state disk drive (SSD) and microelectronic package was performed using the anisotropic viscoelastic shell modeling technique. The thermomechanical properties of various copper patterns were homogenized with the anisotropic shell model, which considered their viscoelastic properties. Then, warpage simulations of an SSD PCB unit/array and a full microelectronic package were performed; these simulations accounted for the initial warpage that occurred during fabrication using ABAQUS combined with a user-defined subroutine. Finally, it was demonstrated that both the maximum warpage and the remaining residual warpage of the full microelectronic package can be accurately predicted.

Index Terms—Anisotropic shell model, initial warpage, microelectronic package, printed circuit board (PCB), warpage simulation.

I. INTRODUCTION

NOWDAYS, many electronic products, such as smartphones, solid-state disk drives (SSDs), or personal digital assistants, are increasingly desired to be lighter, smaller, and have more functions. For these reasons, the circuit density

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of printed circuit boards (PCBs) has been increased using finer electrode lines and thinner cross sections. Also, multilayer PCBs have been extensively used because they can integrate a greater number of complicated circuits compared to single- and double-sided PCBs [1]. Typically, multilayer PCBs consist of woven glass fabric-reinforced epoxy resin, such as bismaleimide triazine, or flame-retardant (FR) substrates sandwiched between copper (Cu) circuits and a photoimageable solder resist (PSR). Therefore, thermally induced warpage of multilayer PCBs can be easily generated during high-temperature reflow processes due to the mismatched coefficient of thermal expansion (CTE) values of each layer. The thermally induced warpage of multilayer PCBs should be accounted for during manufacturing processes to ensure the reliability of the electronic product because warpage can cause significant problems such as solder paste bridging and opening, damage and misconnection of components, cracking of solder joints, and line jams during production [2]. For these reasons, several studies have been carried out using finite-element analysis (FEA) to predict the warpage of multilayer PCBs. In some reports, the mechanical properties of PCBs have been represented by homogenized models because the Cu circuits in PCB layers are too thin and too complicated to simulate with fully meshed elements. Therefore, the Cu circuits of PCBs are sometimes represented by isotropic [3]–[5] or orthotropic elastic plate models [6]–[9]. Also, a relevant study was performed in which various Cu patterns were modeled with anisotropic viscoelastic models because time and temperature are the representative variables during the manufacturing process; thus, viscoelasticity is a very important property that affects the warpage of PCBs [10]. However, in previous works, this viscoelastic warpage simulation has been performed for only flexible thin multilayer PCBs. Therefore, the results from previous modeling methods are limited in their application to the various structures of multilayer PCBs. Also, a viscoelastic warpage simulation technique that accounts for the initial warpage that occurs before the reflow process of PCBs has not been studied. In addition, the initial warpage that occurred during fabrication should be considered in order to perform

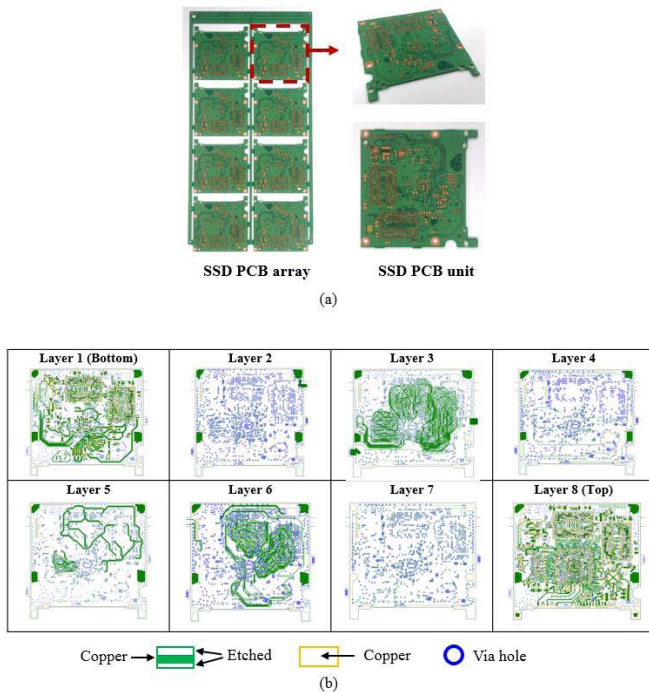


Fig. 1. Multilayer SSD PCB array/unit. (a) Pictures of SSD PCB array and unit. (b) Information of Cu circuits in SSD PCB unit.

accurate warpage simulations; it has been reported that the final warpage deformation of PCBs is significantly affected by their initial warpage state [11], [12].

The aim of this paper is to develop a more accurate and reliable viscoelastic warpage simulation technique in order to predict the warpage behavior of the various structures of multilayer PCBs. In this paper, warpage simulations for an SSD PCB unit/array and a full microelectronic package were performed using the anisotropic viscoelastic shell modeling technique, which takes into consideration the initial warpage. The thermomechanical properties of various Cu patterns were homogenized with the anisotropic shell model by accounting for their viscoelastic properties. Also, the initial warpage was modeled based on the results of a Shadow Moiré experiment using the element reactivation technique. Then, warpage simulations were performed using ABAQUS combined with a user-defined subroutine. The warpage results from the reflow process were compared to those from the Shadow Moiré experiment to verify the developed analysis technique.

II. WARPAGE SIMULATION

A. Anisotropic Viscoelastic Shell Modeling Technique

In this paper, the anisotropic viscoelastic shell modeling technique [10] was used to predict the warpage of high-density SSD PCBs and multilayer PCBs with microelectronic packages. The pictures and layer information of the SSD PCBs used in this paper are shown in Fig. 1(a) and Table I, respectively. The SSD PCB is composed of eight etched Cu circuit layers sandwiched between woven glass fabric-reinforced FR epoxy resin (FR-4) substrates. PSR layers are used to cover the top and bottom of the SSD PCBs.

TABLE I
LAYER INFORMATION OF MULTILAYER SSD PCBs

Layer	Thickness (μm)	Layer	Thickness (μm)
Bottom PSR	20	Circuit layer 5	35
Circuit layer 1	35	FR-4	175
FR-4	65	Circuit layer 6	35
Circuit layer 2	35	FR-4	75
FR-4	75	Circuit layer 7	35
Circuit layer 3	35	FR-4	65
FR-4	175	Circuit layer 8	35
Circuit layer 4	35	Top PSR	20
FR-4	75	Total	1025

The thickness of each Cu circuit layer is $35 \mu\text{m}$, and the thicknesses of the FR-4 substrates are varied from 65 to $175 \mu\text{m}$. As shown in Fig. 1(b), the Cu on the first, third, fifth, sixth, and eighth circuit layers was etched and covered by FR-4 with different shapes and a variety of thicknesses, directions, and patterns. In the case of the SSD PCB array, eight SSD PCB units were attached with the outer frame, which had the same layer composition as the SSD PCB unit [Fig. 1(a)]. The circuit layers in the outer frame were not etched; thus, they were composed of only Cu. The SSD PCB specimen and circuit information were provided by SAMSUNG Electronics. Detailed information about the Cu patterns in the circuit layers is described in Section II-B. The Cu circuits in SSD PCBs are too small and complicated to represent all of the circuits individually in the simulation model. Therefore, in this paper, the viscoelastic pattern modeling technique was adopted; this is based on the effective thermomechanical properties of the Cu circuits, which were determined in [10]. Fig. 2 shows the steps used to model the multilayer PCB with the anisotropic viscoelastic shell modeling technique. First, each Cu circuit layer was discretized with the same size and the representative pattern shapes for Cu were selected. Then, the effective thermomechanical properties of each representative pattern for the equivalent material models were obtained; these properties were assigned to their corresponding areas. Finally, the entire PCB structure, including the FR-4 and PSR layers, was modeled, and the warpage simulation was performed under the reflow temperature. The details of the warpage simulation procedures are described in Section II-C.

B. Obtaining Effective Thermomechanical Properties of the Cu Patterns

In this paper, representative Cu patterns were selected based on the circuit design, and their thermomechanical properties were obtained using FEA. From [10], it was found that the Cu patterns of multilayer PCBs can be divided into three major types: line patterns, Cu-based patterns, and matrix (i.e., the material that covers the circuit layer)-based patterns. All of the circuit layers can be represented by a combination of these patterns. Fig. 3 shows the geometry and FEA models of representative Cu patterns selected for the SSD PCBs. The geometric properties of the Cu patterns were determined from the drawings of the circuit layers, which were provided by

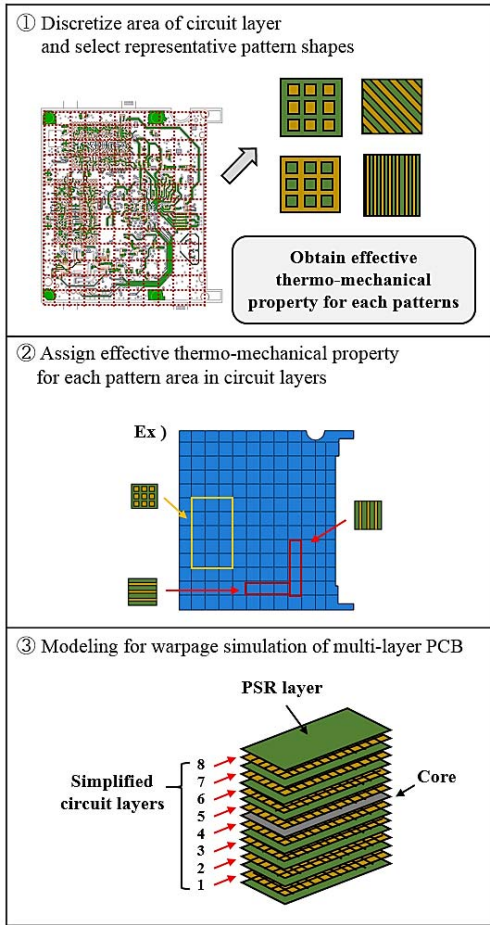


Fig. 2. Steps for anisotropic shell modeling technique for warpage simulation of multilayer PCBs.

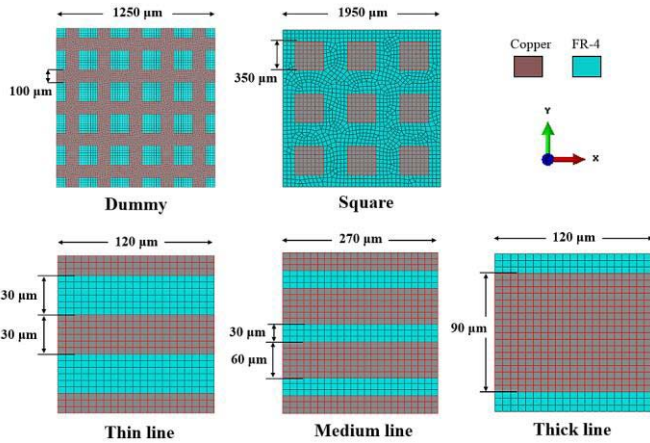


Fig. 3. Finite-element models for effective thermomechanical property of Cu unit pattern.

Samsung Electronics. In this paper, all of the unit pattern models were composed of Cu and FR-4. Therefore, the effective viscoelastic properties of the Cu unit pattern, which consist of an elastic material (Cu) and a viscoelastic material (FR-4), can be modeled as the matrix relaxation moduli of the Cu/FR-4 composite. To obtain the thermomechanical properties of the unit patterns, the viscoelastic properties of FR-4 (and PSR) were represented with a Prony series. Using the Prony series, the relaxation modulus of the viscoelastic material is

TABLE II
RELAXATION TIMES AND RELAXATION COEFFICIENTS OF PCB MATERIALS

i	ρ_i	FR-4	PSR	Copper
		E_i (GPa)		
∞	-	8.197	0.177	53.4
1	1.0×10^{-6}	5.91×10^{-4}	5.83×10^{-2}	-
2	1.0×10^{-5}	6.91×10^{-4}	4.63×10^{-2}	-
3	1.0×10^{-4}	3.91×10^{-5}	5.09×10^{-2}	-
4	1.0×10^{-3}	8.91×10^{-5}	6.69×10^{-2}	-
5	1.0×10^{-1}	5.91×10^{-4}	6.90×10^{-2}	-
6	1.0×10^1	2.79×10^{-4}	2.44×10^{-5}	-
7	1.0×10^3	1.373	0.839	-
WLF constants	T_0 (K)	348	348	
	C_1	4.455	12.053	
	C_2	208.65	274.53	

represented as

$$E(t) = E_\infty + \sum_{i=1}^n E_i e^{-t/\rho_i} \quad (1)$$

where t is the time, E_∞ is the long-term modulus, E_i denotes the Prony coefficients, and ρ_i denotes the relaxation times. Also, the time-temperature shift factor is expressed in terms of the Williams-Landel-Ferry (WLF) equation as

$$\log a_T = -\frac{c_1(T - T_0)}{c_2 + (T - T_0)} \quad (2)$$

where c_1 and c_2 are the material constants that depend on the particular material and the logarithm is base 10. T_0 is the reference temperature, and a_T is the shift factor, which expresses the ratio of relaxation times between the reference temperature and the specific temperature T

$$a_T = \frac{\rho(T)}{\rho(T_0)} \quad (3)$$

where ρ is the relaxation time. The viscoelastic properties of FR-4 and PSR were obtained with vibration tests [13], and their relaxation master curves and parameters of the Prony series are represented in Fig. 4(a) and Table II, respectively. Also, the temperature-dependent CTEs of FR-4 and PSR were accounted for, as shown in Fig. 4(b). These were provided by Samsung Electronics. Using the thermomechanical properties of PCB materials, the effective thermomechanical properties of the Cu unit patterns can be directly obtained from the FEA. This approach was adopted based on the report of Brinson and Knauss [14], which calculated the effective viscoelastic properties of a unidirectional fiber composite. In the case of an anisotropic line pattern, the constitutive relationships for the homogenized shell are described as

$$\begin{aligned} [N(t)] &= \int_0^t ([A(t-s)][\dot{\epsilon}(s)] + [B(t-s)][\dot{\kappa}(s)]) ds \\ [M(t)] &= \int_0^t ([B(t-s)][\dot{\epsilon}(s)] + [D(t-s)][\dot{\kappa}(s)]) ds. \end{aligned} \quad (4)$$

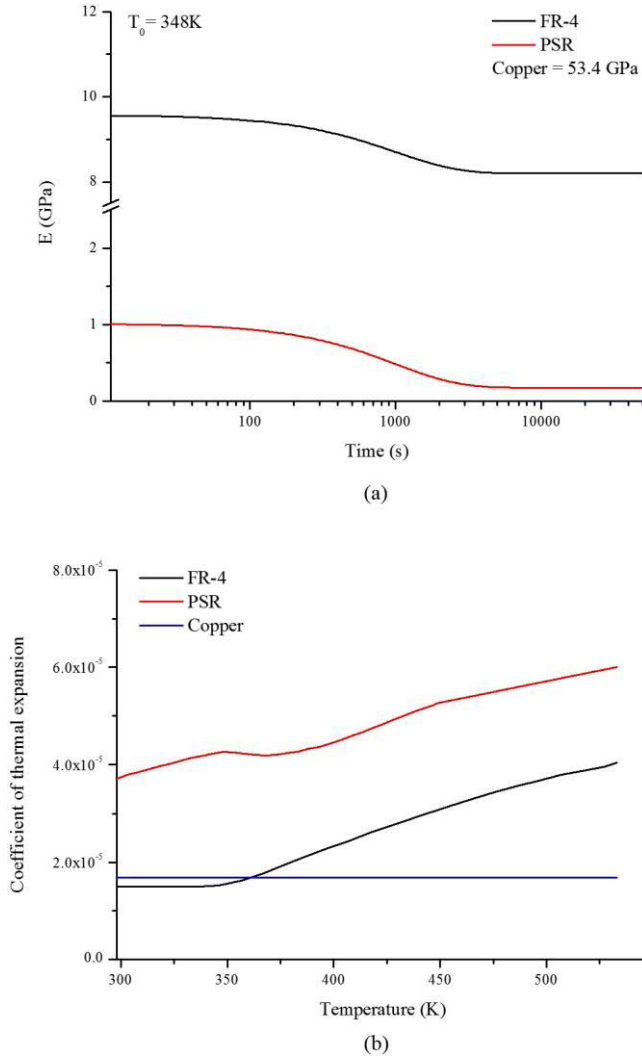


Fig. 4. Mechanical properties of PCB materials. (a) Viscoelastic master curves at a reference temperature of $T_0 = 348$ K. (b) Temperature-dependent CTEs.

Here, the matrix $[N]$ is the force, $[M]$ is the moment, and $[\varepsilon]$ and $[\kappa]$ denote the midplane strains and out-of-plane curvatures, respectively. The matrices $[A]$, $[B]$, and $[D]$ represent the in-plane stiffness, stretching-bending coupling, and bending stiffness matrices, respectively, which are typically used in composite shell modeling in classical laminate theory [15]. They are combined to give the ABD stiffness matrix, as follows:

$$ABD(t) = \begin{bmatrix} A_{11}(t) & A_{12}(t) & A_{16}(t) & B_{11}(t) & B_{12}(t) & B_{16}(t) \\ A_{21}(t) & A_{22}(t) & A_{26}(t) & B_{21}(t) & B_{22}(t) & B_{26}(t) \\ A_{61}(t) & A_{62}(t) & A_{66}(t) & B_{61}(t) & B_{62}(t) & B_{66}(t) \\ B_{11}(t) & B_{12}(t) & B_{16}(t) & D_{11}(t) & D_{12}(t) & D_{16}(t) \\ B_{21}(t) & B_{22}(t) & B_{26}(t) & D_{21}(t) & D_{22}(t) & D_{26}(t) \\ B_{61}(t) & B_{62}(t) & B_{66}(t) & D_{61}(t) & D_{62}(t) & D_{66}(t) \end{bmatrix}. \quad (5)$$

For anisotropic line patterns, three virtual tests are needed for the x -, y -, and xy -directions in order to acquire the independent time-varying functions in $ABD(t)$. Virtual relaxation

tests were performed by stretching each edge to a strain of 0.005 over 1 s and then holding for 105 s. Periodic displacement boundary conditions were applied between each pair of opposite boundary edges of the unit cells for all of these analyses. The CTE of each material was not included in order to remove the effects of expansion caused by temperature. The temperature was set to 348 K, which is the reference temperature for the WLF constants of FR-4 (see Table I). The viscoelastic master curve of the unit patterns can be directly obtained at this temperature, and the WLF constants are the same as those of FR-4 because Cu has only elastic properties. For the same reason, all of the constituents of the $ABD(t)$ matrix can be modeled with the same relaxation times as those of FR-4 [16]. Then, the reduced stiffness matrix $[Q(t)]$ can be calculated from the results of the stress relaxation tests $[E_x(t)$, $E_y(t)$, and $G_{xy}(t)]$, as follows:

$$[Q(t)] = \begin{bmatrix} \frac{E_x(t)}{1 - \nu_{12}\nu_{21}} & \frac{\nu_{12}E_y(t)}{1 - \nu_{12}\nu_{21}} & 0 \\ \frac{\nu_{12}E_y(t)}{1 - \nu_{12}\nu_{21}} & \frac{E_y(t)}{1 - \nu_{12}\nu_{21}} & 0 \\ 0 & 0 & G_{xy}(t) \end{bmatrix} \quad (6)$$

where ν_{12} and ν_{21} are the major and minor Poisson's ratios of the unit pattern that are obtained from the virtual relaxation tests. In this paper, in order to simplify the calculation, Poisson's ratios are assumed to be constant values. The effect of Poisson's ratio is expected to be minor because the bending behavior of the unit shells is primarily 1-D [17]. Based on the result of $[Q(t)]$, the corresponding constituents of $[A(t)]$ and $[D(t)]$ can be obtained using the following equations [15]:

$$\begin{aligned} [A(t)] &= [Q(t)] \times t \\ [D(t)] &= [Q(t)] \times t^3/12 \end{aligned} \quad (7)$$

where t is the thickness of the Cu circuit layer. By numerical fitting with respect to time, the Prony coefficients of each of the constituents of $ABD(t)$ for thin, medium, and thick line patterns can be determined. For the dummy and square patterns, the viscoelastic properties were homogenized by the isotropic shell because they have the same shapes as Cu in both the x - and y -directions; thus, the anisotropic effects were negligible (see Fig. 3). For these patterns, the viscoelastic properties were determined by performing the representative virtual relaxation test for just the x -direction.

Also, the CTEs of each unit pattern were obtained by virtual thermal expansion tests. In this paper, a temperature change from 298 to 450 K was applied to the FEA model of the unit pattern. During the virtual CTE tests, only the CTE and elastic properties of FR-4 and Cu were included in the model; this was done to remove the viscoelastic effects during simulation. Similar to the method used to determine the viscoelastic properties, simulations were performed in the x - and y -directions (for the line patterns) and in only the x -direction (for the dummy and square patterns).

C. Finite-Element Analysis Model of Multilayer SSD PCBs

The discretized map of SSD PCB circuit layers, based on their pattern, is shown in Fig. 5. Based on this mapping, the

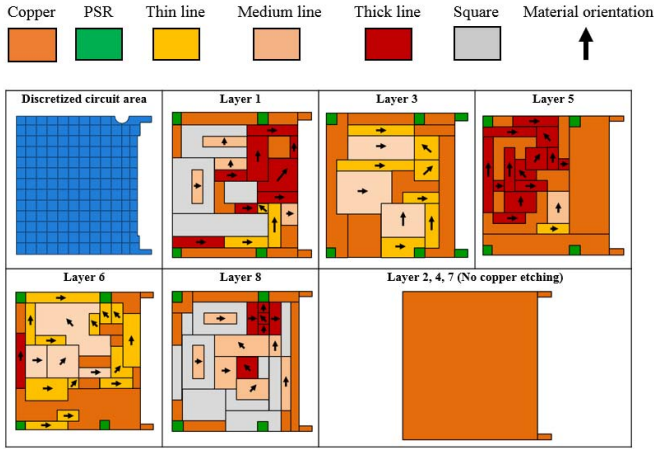


Fig. 5. Discretized pattern area of circuit layers of SSD PCB unit.

thermomechanical properties of the Cu patterns obtained from Section II-A were assigned to each area. For line patterns, the material orientation should be considered because of the anisotropic viscoelastic properties. The anisotropic viscoelastic stiffness properties were defined by assigning the $ABD(t)$ matrix via a user-defined shell section subroutine (UGENS) with the material orientation. Finally, the thermomechanical properties of circuit layers can be simply defined; thus, the entire SSD PCB model can also be simplified. The SSD PCB unit and array were modeled and meshed with 10370 and 116399 reduced integration four-node shell elements (S4R), as shown in Fig. 6(a) and (b), respectively. All of the layers were meshed by the same shapes to ensure stability of convergence and to reduce the simulation time. It is noteworthy that only 116399 elements are needed for warpage simulation of the entire SSD PCB array, which consists of eight multilayer SSD PCBs (including the complicated Cu circuits). It has been reported that more than 50 times as many elements may be needed to model SSD PCBs using conventional modeling techniques that account for each of the Cu circuits [10]. Therefore, when using a conventional modeling technique, the viscoelastic warpage simulation is almost impossible due to its large computation size and the accompanying data storage requirements.

As shown in Fig. 6(a) and (b), the SSD PCB unit and array were assembled on the rigid ground, and a gravity load was applied during simulation. The gaps between each of the layers were determined based on their thicknesses, and the interfaces between each of the layers were constrained to have perfect bonding; this was done with the *TIE function in ABAQUS. Also, a frictionless contact interaction was allowed between the bottom PSR layer and the ground through the *SURFACE INTERACTION command. In addition, movement constraints were applied in the x -direction, the y -direction, and the rotational freedom for the z -direction to the center node in the middle FR-4 layer. Then, the initial warpage that occurred during fabrication of the multilayer PCB was accounted for in the FEA in order to obtain accurate results in the warpage simulation. For example, the warpage mechanism of bilayer structure during heating process was represented as shown in Fig. 7, where α_1 and α_2 denote their CTEs, E_1 and E_2

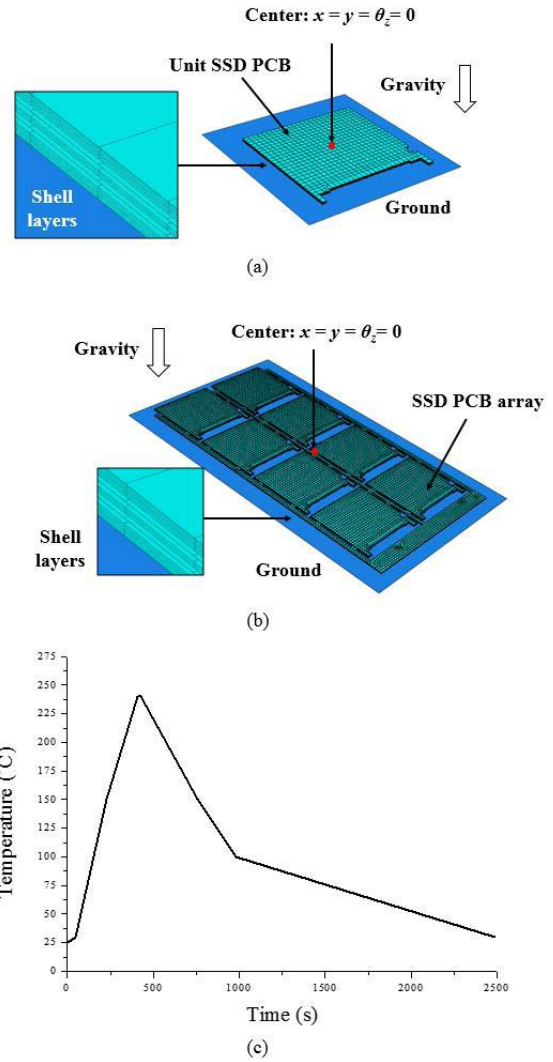


Fig. 6. Finite-element model of SSD PCBs for warpage simulation. (a) SSD PCB unit. (b) SSD PCB array. (c) History of reflow temperature.

are their modulus of elasticity, t_1 and t_2 are their thickness, and h is the total thickness, respectively. If α_2 is bigger than α_1 , the deflection will be convex down by change of temperature (ΔT) as shown in Fig. 7(b). All the forces acting over the section of material₁ on the concave side can be represented by an axial tensile force P_1 and bending moment M_1 . For material₂ on the convex side, all forces acting on the cross section can be represented by an axial compressive force P_2 and bending moment M_2 . Due to the axial force and bending moment, the stress distribution is produced along the interface between two layers as shown in Fig. 7(c). In this case, the curvature ($1/\rho$) of bilayer structure can be obtained from the fact that the all forces acting over any cross section of the strip must be equilibrium, as follows [18]:

$$\frac{1}{\rho} = \frac{6(\alpha_2 - \alpha_1)(\Delta T)(1 + m)^2}{h \left(3(1 + m)^2 + (1 + mn) \left(m^2 + \frac{1}{mn} \right) \right)}, \quad m = t_1/t_2, \quad n = E_1/E_2. \quad (8)$$

However, this analysis can be used with the assumption that the cross sections of the structure are originally plane.

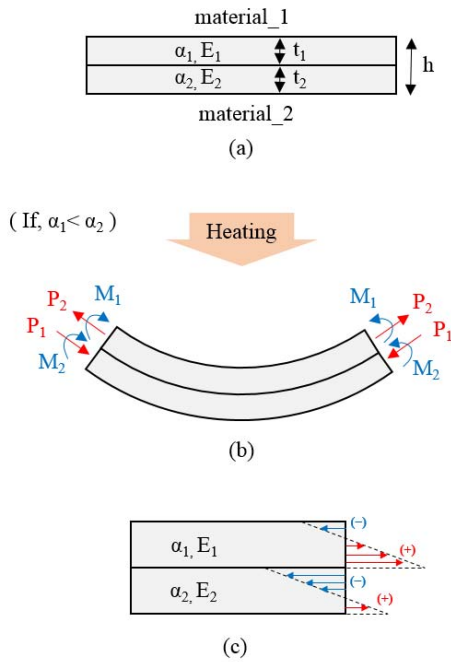


Fig. 7. Warpage of simple bilayer structure. (a) Bilayer structure. (b) Warpage during heating process. (c) Stress distribution while heating.

The force moment and stress distribution is changed according to the initial warpage state of PCB due to the noncoplanarity. Also, because the warpage behavior is affected by the moduli, this effect should be larger in multilayer PCB that has complex structure with viscoelastic materials. In other words, because the initial warpage influences on the force and stress distribution in each layer and the transition of moduli in viscoelastic material, the warpage behavior of entire PCB should be changed during high temperature compared to the nonwarpage case. Therefore, the initial warpage should be accounted for accurate prediction of warpage because these effects cannot be determined in an elementary way for multilayer PCB. It has been reported that the final warpage deformation is affected by the initial warpage state [12], [13].

In general, the initial warpage of multilayer PCBs is increased as the number of circuit layers and the size increase; this is the case because the initial warpage is generated during the manufacturing process by the mismatched CTEs between each layer. For example, it was found that the SSD PCB unit/array and microelectronic package used in this paper have almost the same amount (or a greater amount) of initial warpage compared to the warpage generated during high-temperature reflow (this was determined by the Shadow Moiré experiment described in Section III). In this paper, the initial warpage of the SSD PCBs was applied to the FEA model before the reflow temperature using the element reactivate technique, as shown in Fig. 8. After displacement was applied to the nodes to model the initial warpage, all of the elements for the PCB were deactivated and reactivated with no strain using the *MODEL CHANGE command in ABAQUS in order to remove the stress components of the elements. Using this technique, the FEA model of PCB has only the displacement distribution as the initial warpage (without the

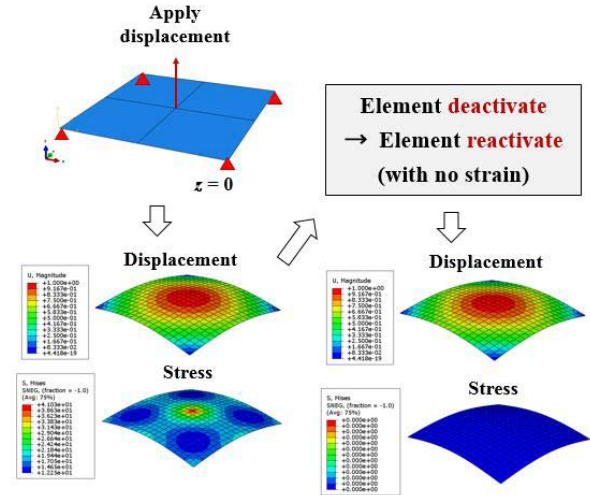


Fig. 8. Modeling procedure of the initial warpage in FEA using element reactivate technique.

internal stress). In this paper, the initial warpage was applied to PCB models based on the data measured with the Shadow Moiré experiment. Then, quasi-static analyses were carried out using the *VISCO step of ABAQUS and the reflow temperature profile, as shown in Fig. 6(c). The temperature history was also described based on the data measured from the warpage experiment using the Shadow Moiré method. In addition, for comparison, warpage simulation was performed without accounting for the initial warpage.

The full microelectronic package, with a multilayer PCB, was also analyzed in the same manner. Fig. 9(a) shows the structure of the target PCB, which consisted of a semiconductor chip/electromagnetic compatibility (EMC) portion and a multilayer PCB portion. As shown in Fig. 9(b), the semiconductor chip and EMC were modeled, and the elastic and viscoelastic mechanical properties were assigned, respectively, based on product information supplied by Samsung Electronics. All interfaces between the semiconductor chips and EMC were constrained to have perfect bonding; this was done using the *TIE and *SHELL TO SOLID COUPLING commands. In the case of the multilayer PCB portion, the anisotropic viscoelastic pattern modeling technique was used with the same modeling procedure that was used for SSD PCBs, as shown in Fig. 9(c) (detailed circuit information is not included due to the security requirements of the company). After assembling the chip/EMC and multilayer PCB portions with the *TIE constraint, the entire model was meshed with 13 746 reduced integration four-node shell elements (S4R) and 3464 reduced integration eight-node solid elements (C3D8R), as shown in Fig. 9(d). Then, quasi-static analysis was performed with the reflow temperature [Fig. 6(c)] for the warpage simulation. Also, the initial warpage was accounted for before the reflow process simulation in order to investigate the effects of the initial warpage.

III. SHADOW MOIRÉ EXPERIMENT

The warpage of multilayer PCBs and full microelectronic packages during the reflow process was measured by the

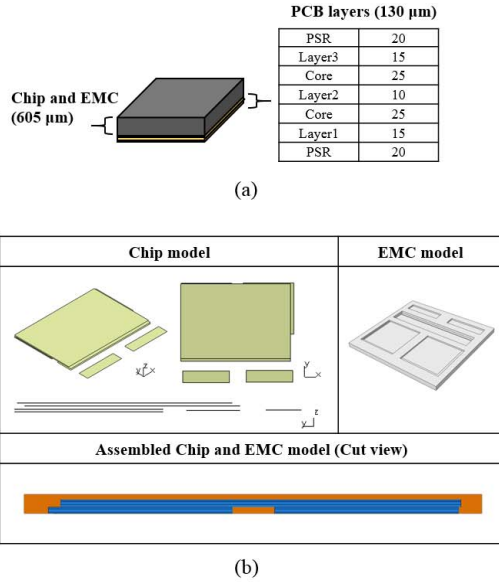


Fig. 9. Warpage simulation of PCB/microelectronic package. (a) Schematic of specimen and layer information. (b) Modeling of semiconductor chips and EMC part. (c) Pattern area modeling of PCB layers. (d) Finally assembled and meshed PCB/microelectronic package FEA model.

Shadow Moiré test. The Shadow Moiré technique measures the topography of the surface from a planar surface [19]. Fig. 10(a) and (b) shows the Shadow Moiré equipment (TherMoiré AXP, Akrometrix, USA) and the mounted SSD PCB unit/array specimens, which were spray-treated to be white to obtain exact warpage results. The reflow temperature history of the specimens was monitored by a K-type thermocouple (located on the PCB specimen) with a continuous detection system. The precision was ± 1 °C. This temperature history was accounted for in the warpage simulations [Fig. 6(c)].

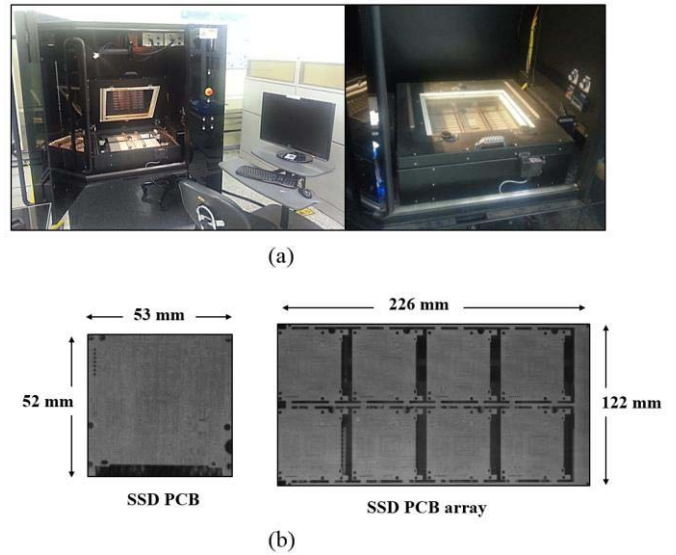


Fig. 10. Experimental setup of Shadow Moiré for PCB warpage observation. (a) Photograph of Shadow Moiré equipment. (b) SSD PCB unit/array specimens mounted on Shadow Moiré.

IV. RESULTS AND DISCUSSION

A. Thermomechanical Properties of Equivalent Circuit Patterns

The equivalent viscoelastic master curves of the Cu patterns of SSD PCBs (Fig. 3), obtained from the virtual relaxation tests at a reference temperature of 348 K, are shown in Fig. 11(a). For the line patterns, the master curves for both the x - and y -directions are depicted in order to compare their anisotropic properties. It was found that the moduli of all Cu patterns decreased as time passed because of the viscoelastic properties of FR-4. It should be noted that the square pattern has the smallest modulus. This was the case because all of the Cu parts were isolated by FR-4 (Fig. 3), which has a lower modulus than that of Cu (53.4 GPa). Similarly, the moduli of line patterns for the y -direction showed smaller values compared to the x -direction; this is due to the isolated Cu parts in the y -direction. Also, it was found that the moduli of these isolated patterns (square and y -direction of the line patterns) were significantly decreased with respect to the time, compared to the other patterns. In the case of the line patterns, the modulus increased as the ratio of the Cu area in the unit pattern was increased. For example, the x -direction of the thick line has the highest modulus because the unit pattern has a higher Cu ratio in the x -direction (75%). In addition, the moduli of line patterns for the x -direction barely decreased as time passed. This is due to the fact that the mechanical properties in the x -direction were dominated by Cu (elastic material) and not by FR-4 (viscoelastic material).

The CTEs of the Cu unit patterns obtained from the virtual expansion tests are shown in Fig. 11(b). Similar to the viscoelastic properties, we found that the CTEs of the square and y -direction of line patterns showed higher values compared to the other patterns; this was due to the higher CTE of FR-4 (from 370 K). It was also caused by the fact that the Cu shapes in their unit patterns were isolated by FR-4.

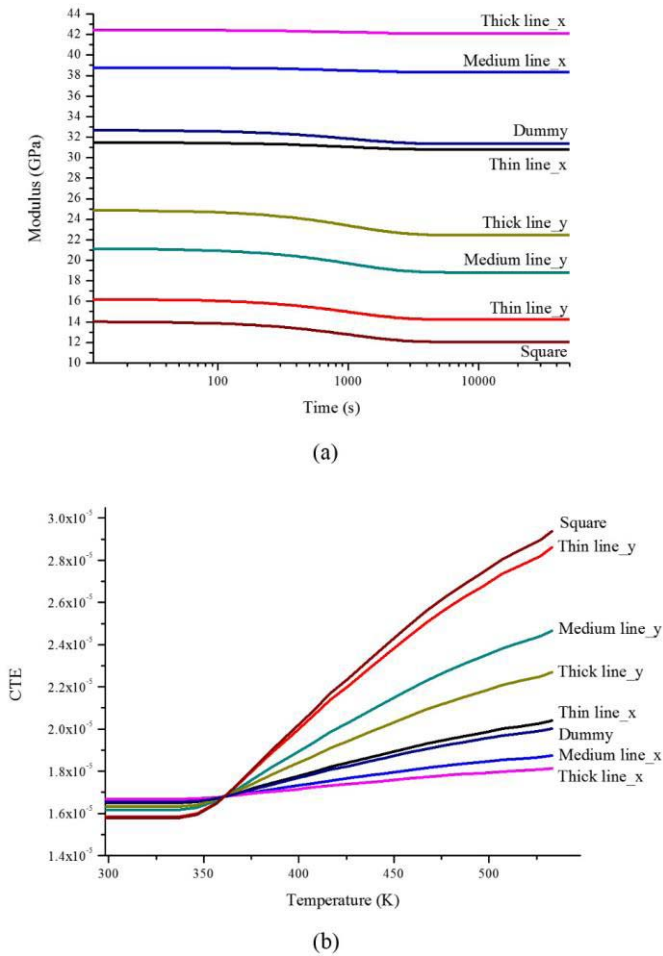
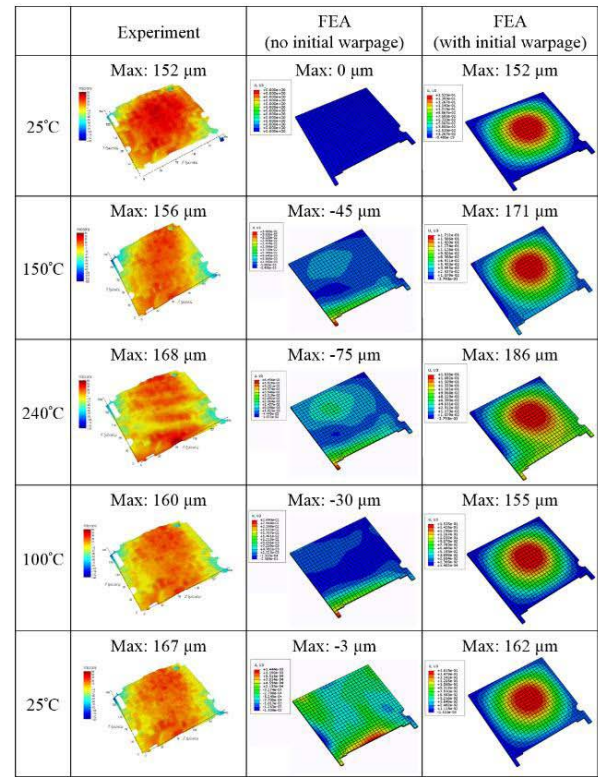


Fig. 11. Thermomechanical properties of Cu patterns obtained from virtual test simulation. (a) Viscoelastic master curves at reference temperature 348 K. (b) Temperature-dependent CTEs.

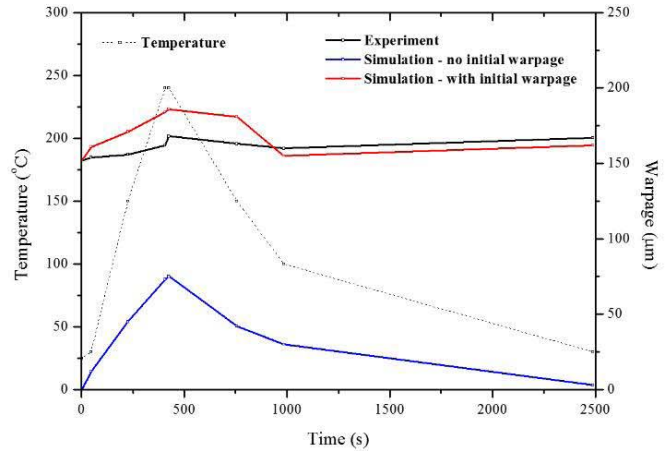
Similarly, the x -direction of the thick line pattern showed almost the same CTE as Cu (1.68×10^{-5}) because the mechanical properties in the x -direction are dominated by Cu. Based on these results, the thermomechanical properties of the Cu patterns can be defined using the Prony coefficients and the temperature-dependent CTE.

B. Warpage of the Multilayer PCBs

Fig. 12 shows the warpages of the SSD PCB unit during the reflow process that was obtained from the Shadow Moiré experiment, the simulation without the initial warpage, and the simulation with the initial warpage, respectively. From the experimental results, it was found that there is significant initial warpage ($152 \mu\text{m}$) in the center area compared to the maximum warpage ($168 \mu\text{m}$) that occurred during the reflow process. Only $16 \mu\text{m}$ of warpage was generated during the reflow process, and $167 \mu\text{m}$ of the residual warpage remained after the reflow process. It is noteworthy that the residual warpage after the reflow process showed a similar value and contour compared to those of the initial warpage. Therefore, it can be seen that the remaining residual warpage is significantly affected by the initial warpage state, although



(a)



(b)

Fig. 12. Warpage results of SSD PCB unit from experiment and simulation with respect to the reflow process. (a) Warpage contours. (b) Maximum warpage during reflow temperature.

some warpage was also generated during the reflow process. As described in Section I, the remaining residual warpage should be predicted for manufacturing processes because it can cause significant problems such as disconnection of solder paste bridging, mismatching with mounted microelectronic packages, or crack generation in solder joints. Unsurprisingly, in the warpage simulation that does not account for the initial warpage, the simulation results showed completely different values and contours compared to the experimental results [warpage occurred in the opposite direction; see Fig. 12(a), middle]. For the warpage simulation that does

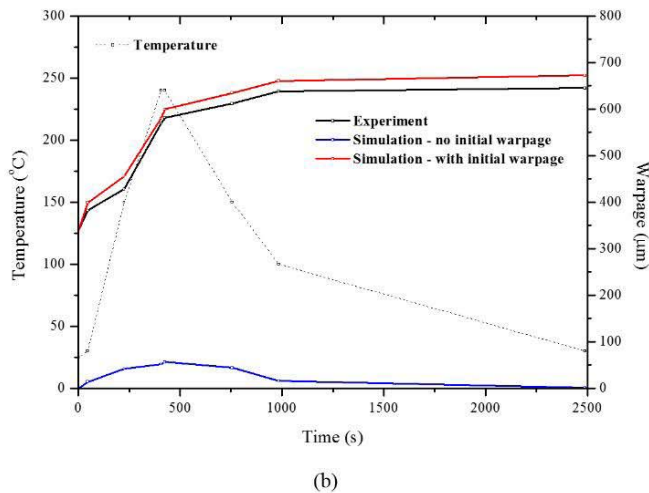
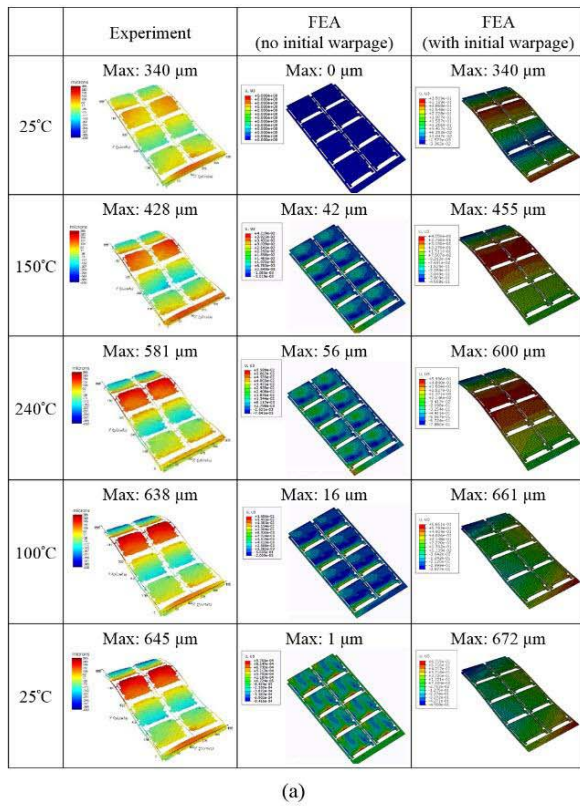


Fig. 13. Warpage results of SSD PCB array from experiment and simulation with respect to the reflow process. (a) Warpage contours. (b) Maximum warpage during reflow temperature.

account for the initial warpage, the simulation results showed good agreement with the experimental warpage values and contours for each temperature point. After warpage was generated up to the maximum temperature (240 °C), it was slightly reduced before increasing again after 1000 s; this trend is similar to the experimental results [Fig. 12(a) and (b)]. This behavior is caused by the fact that the difference in the thermomechanical properties between each layer increased with respect to the time and temperature history due to the viscoelastic properties. Also, it was found that the remaining residual warpage showed a similar contour compared to the initial warpage value (162 μm) and contour were similar

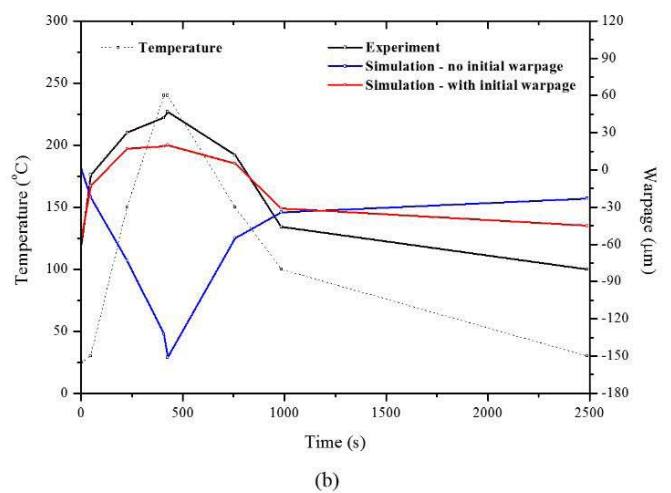
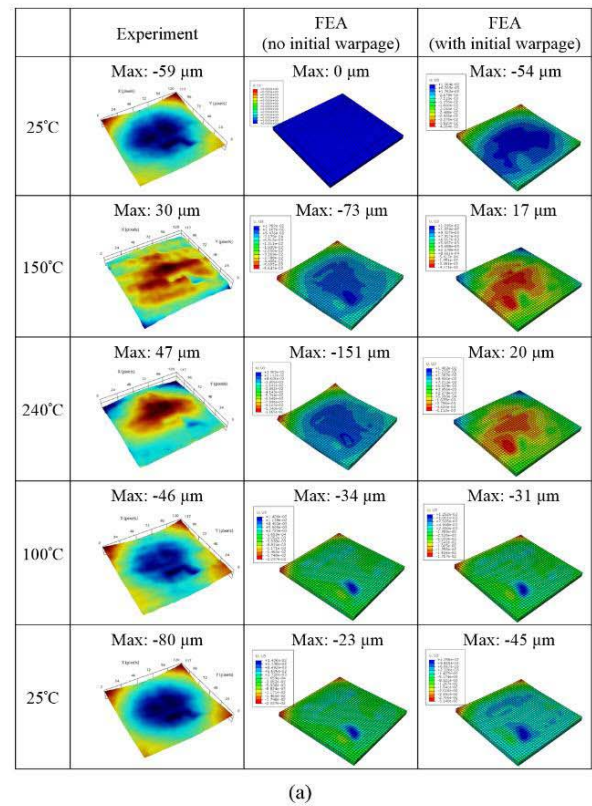


Fig. 14. Warpage results of multilayer PCB with microelectronic package from experiment and simulation with respect to the reflow process. (a) Warpage contours. (b) Maximum warpage during reflow temperature.

to the experimental results (167 μm). From this, it can be determined that the initial warpage has a significant effect on both the reflow warpage and the remaining residual warpage.

The warpages of the entire SSD PCB array during the reflow process, obtained via the Shadow Moiré experiment and simulation, are shown in Fig. 13. From the experimental results, it was found that there was also significant initial warpage (340 μm) compared to the maximum warpage (645 μm), similar to the case of the SSD PCB unit. The remaining residual warpage showed a similar contour compared to the initial warpage, although about 300 μm of warpage was

generated during the reflow process. Also, it can be seen that warpage was continuously generated, despite the fact that the temperature was decreased after 500 s; this is due to the viscoelastic properties of the PCB layers. Similar to the simulation of the SSD PCB unit, good agreement between the simulated and experimental results (in terms of the warpage values and contours) was obtained only when the initial warpage was accounted for in the FEA model. The simulation results that did not consider the initial warpage showed completely different warpage values and contours compared to those of the experimental results.

Fig. 14 shows the warpages of the full microelectronic package with a multilayer PCB during the reflow process that were obtained from the Shadow Moiré experiment and simulation. The experimental results show a large amount of initial warpage ($59\ \mu\text{m}$) in the edge area compared to the value of the maximum warpage after the reflow process ($80\ \mu\text{m}$). As the temperature increases, warpage was generated in the reverse direction of the initial warpage and then warped again in the direction of the initial warpage. This is important information because it implies that the final remaining residual warpage is significantly affected by the initial warpage state (similar to the SSD PCBs). The simulation results that do not consider the initial warpage showed completely different warpage values and contours, compared to the experimental results, while the simulation that considers the initial warpage showed good agreement in terms of the warpage value and the warpage shape [see Fig. 14(a)]. From these results, it can be concluded that both the maximum warpage and the remaining final residual warpage of the various structures of multilayer PCBs and full microelectronic packages can be accurately predicted using the viscoelastic shell modeling technique that accounts for the initial warpage that occurred during fabrication.

V. CONCLUSION

In this paper, warpage simulations for an SSD PCB unit/array and a full microelectronic package with a multilayer PCB were conducted using the anisotropic viscoelastic shell modeling technique that accounts for the initial warpage. The effective thermomechanical properties for various Cu patterns were obtained with the anisotropic shell model, which considered their viscoelastic properties. Finally, it was demonstrated that both the maximum warpage and the remaining residual warpage of multilayer PCBs and microelectronic packages can be accurately predicted using the viscoelastic shell modeling technique that considers the initial warpage. It is expected that the simulation technique developed in this paper can be widely used to predict warpage in various multilayer PCB products.

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